CMS42N10H8-HF

N-Channel
RoHS Device
Halogen Free

Description

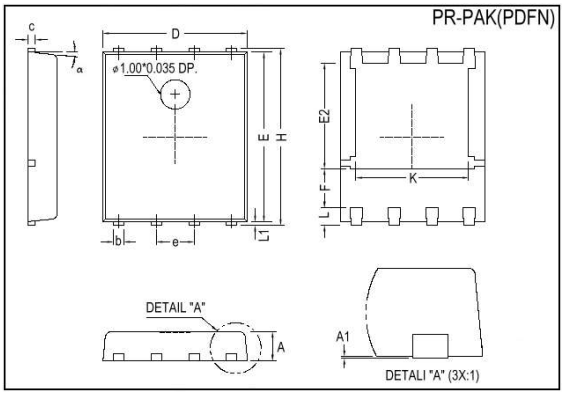
The CMS42N10H8 uses advanced Trench technology and designs to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

The CMS42N10H8 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

Low On-Resistance
Low Input Capacitance
Green Device Available
Low Miller Charge
100% EAS Guaranteed

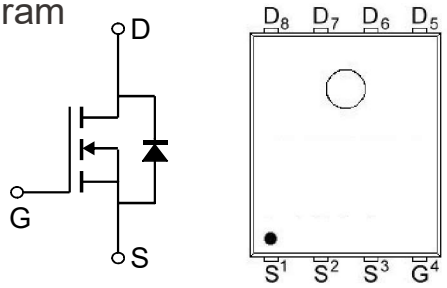
Package Dimensions



REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.85	1.00	1.15	E	5.70	-	5.90
A1	0.00	-	0.10	e	-	1.27	-
b	0.30	-	0.51	H	5.90	-	6.20
c	0.20	-	0.30	L	-	0.60	-
D	4.80	-	5.00	L1	0.06	-	0.20
F	1.10REF.			α	0°	-	12°
E2	3.50REF.			K	3.70	3.90	4.10

Circuit diagram

- G : Gate
- S : Source
- D : Drain



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current[1]	I_D @T_C=25℃	42	A
	I_D @T_C=70℃	34	A
Pulsed Drain Current[1]	I_{DM}	150	A
Continuous Drain Current	I_D @T_A=25℃	6.6	A
	I_D @T_A=70℃	5.3	A
Total Power Dissipation	P_D @T_C=25℃	83.3	W
	P_D @T_A=25℃	3.6	W
Single Pulse Avalanche Energy, L=3mH	E_{AS}	63	mJ
Single Pulse Avalanche Current, L=3mH	I_{AS}	6.5	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	℃

Thermal Data

Parameter	Symbol	Conditions	Max. Value	Unit
Thermal Resistance Junction-ambient[2]	$R_{\theta JA}$	Steady State	35	℃/W
Thermal Resistance Junction-case[2]	$R_{\theta JC}$	Steady State	1.5	℃/W

Electrical Characteristics (T_J = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	100	-	-	V	V_{GS}=0, I_D =250uA
Gate Threshold Voltage	$V_{GS(th)}$	1.2	1.8	2.5	V	V_{DS}=V_{GS}, I_D=250uA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	I_{DSS}	-	-	1	uA	V_{DS}=80V, V_{GS}=0
Static Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	20	25	mΩ	V_{GS}=10V, I_D=10A
		-	22	28.5		V_{GS}=4.5V, I_D=10A
Total Gate Charge [1]	Qg	-	34	-	nC	I_D=10A V_{DS}=50V V_{GS}=10V
Gate-Source Charge	Qgs	-	6	-		
Gate-Drain ("Miller") Change	Qgd	-	9	-		
Turn-on Delay Time [1]	$T_{d(on)}$	-	7	-	ns	V_{DS}=50V V_{GS}=10V R_G=3Ω R_L=5Ω
Rise Time	T_r	-	7	-		
Turn-off Delay Time	$T_{d(off)}$	-	29	-		
Fall Time	T_f	-	7	-		
Input Capacitance	Ciss	-	1325	-	pF	V_{GS}=0V V_{DS}=30V f=1.0MHz
Output Capacitance	Coss	-	110	-		
Reverse Transfer Capacitance	Crss	-	64	-		

Guaranteed Avalanche Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy [3]	EAS	34.5	-	-	mJ	V_{DD}=50V, L=3mH, I_{AS}=4.8A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage	VSD	-	-	1.3	V	I_S=10A, V_{GS}=0V
Reverse Recovery Time	trr	-	32	-	ns	I_F=10A, dI/dt=500A/μs, T_J=25°C
Reverse Recovery Charge	Qrr	-	200	-	nC	

Notes: 1. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.

3. The Min. value is 100% EAS tested guarantee.

TYPICAL CHARACTERISTIC

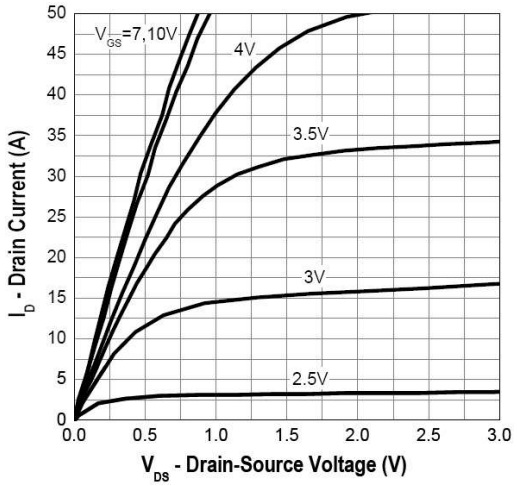


Fig.1 Typical Output Characteristics

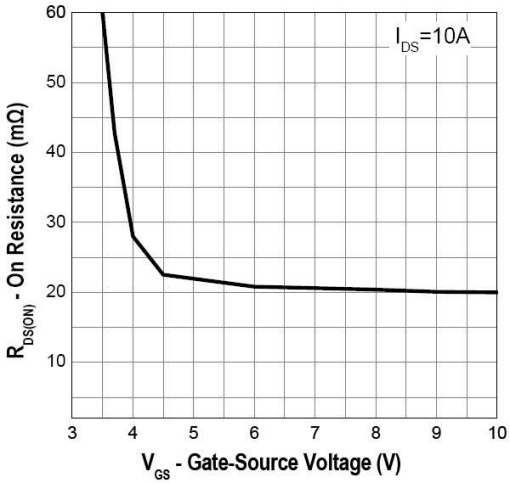


Fig.2 On-Resistance vs. G-S Voltage

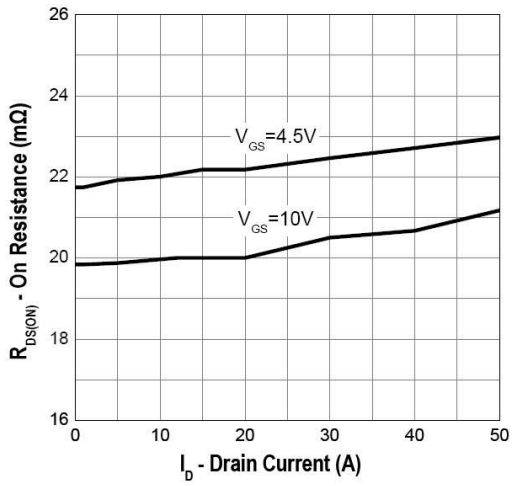


Fig.3 On-Resistance vs. Drain Current

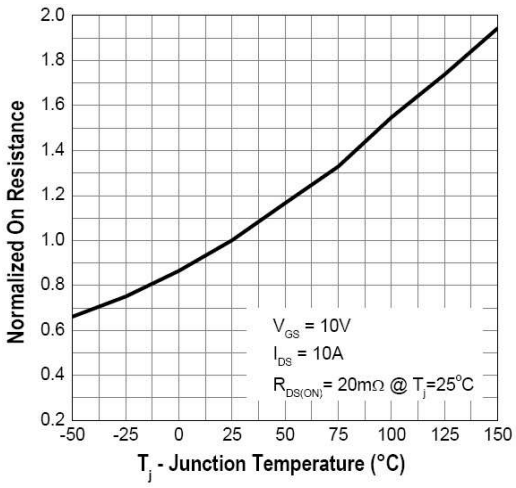


Fig.4 Normalized R_{DSON} vs. T_J

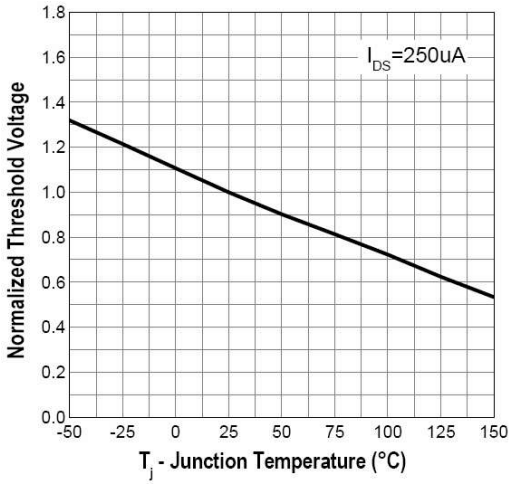


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

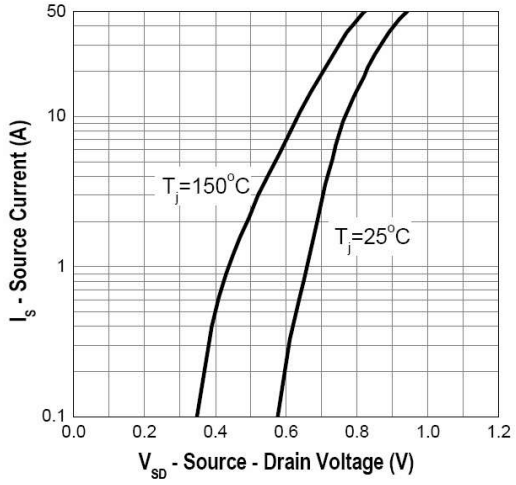


Fig.6 Forward Characteristics of Reverse

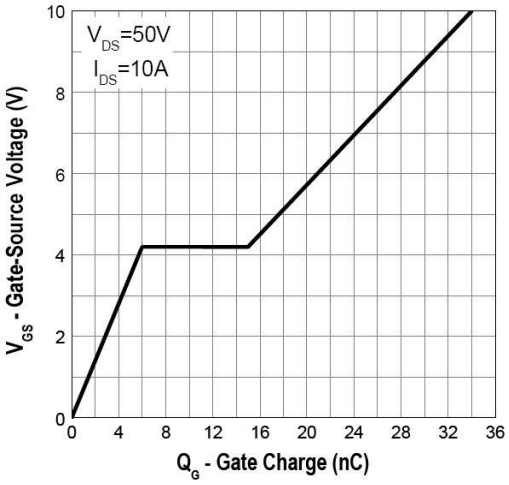


Fig.7 Gate Charge Characteristics

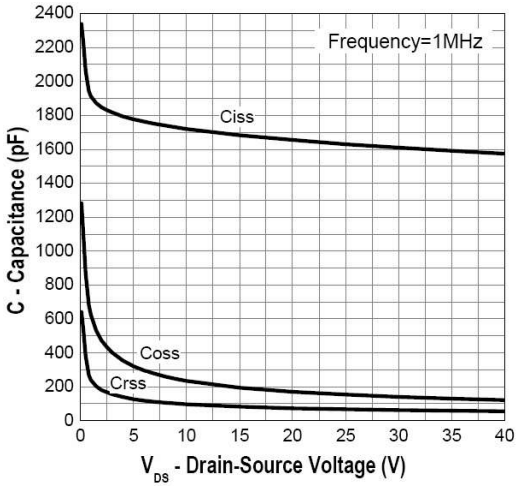


Fig.8 Capacitance Characteristics

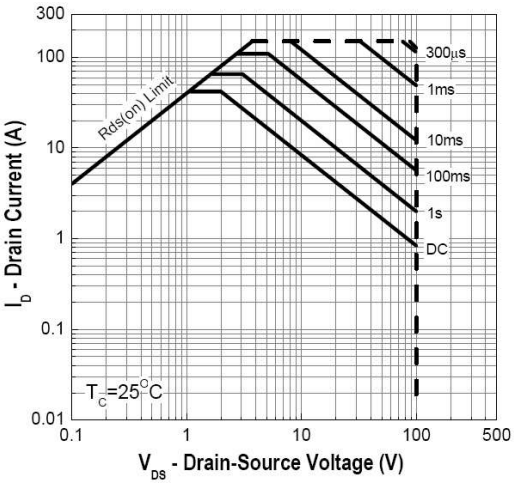


Fig.9 Safe Operating Area

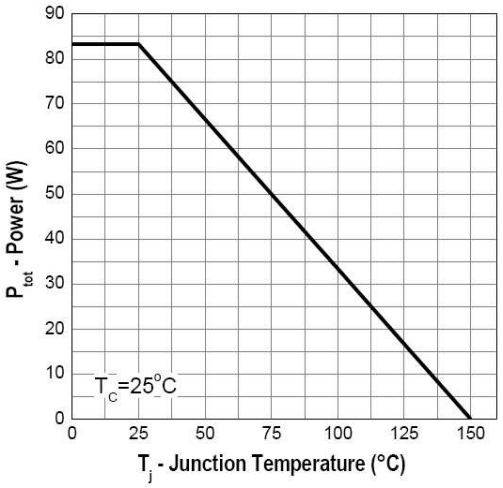


Fig.10 Power Dissipation

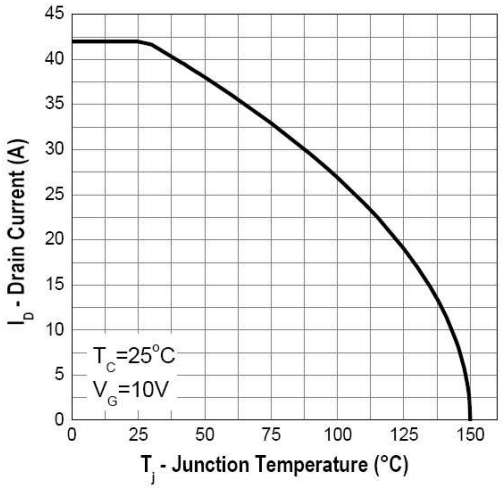


Fig.11 Drain Current vs. T_J

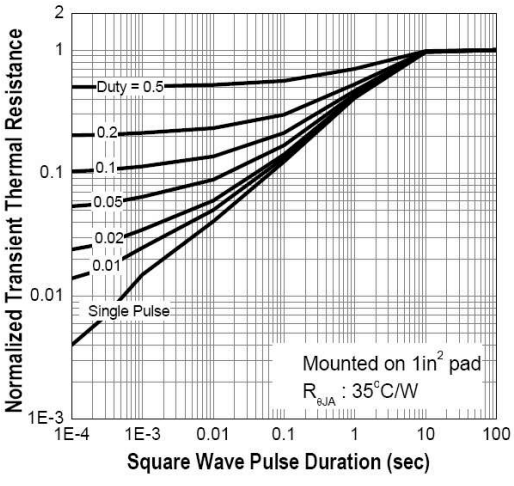
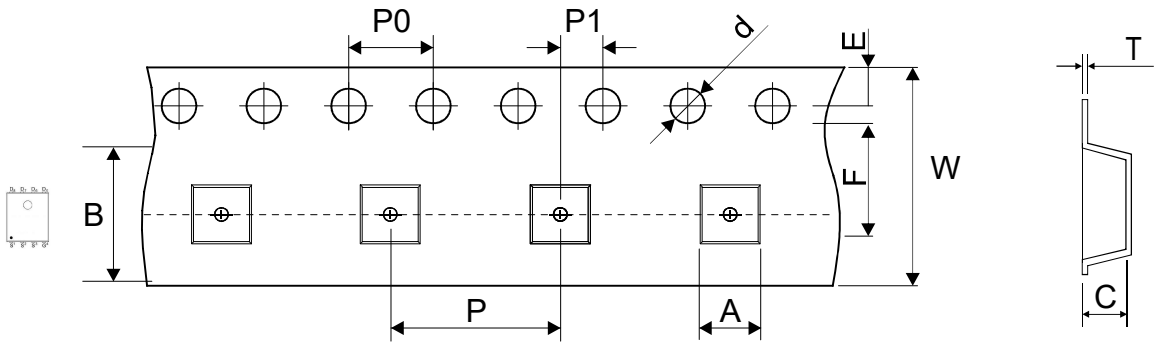
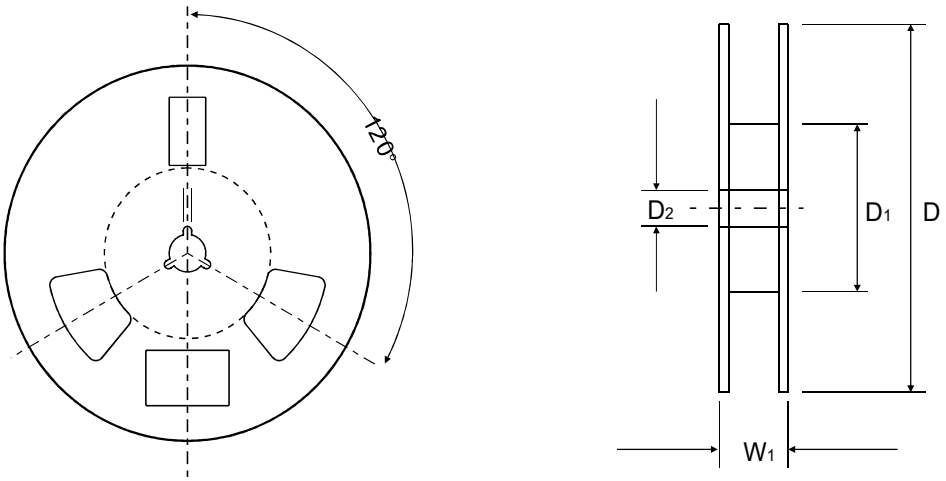
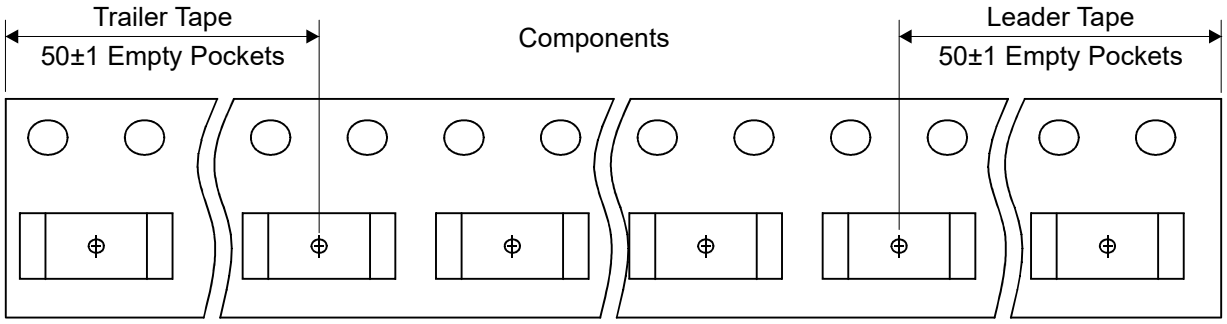


Fig.12 Transient Thermal Impedance

Reel Taping Specification







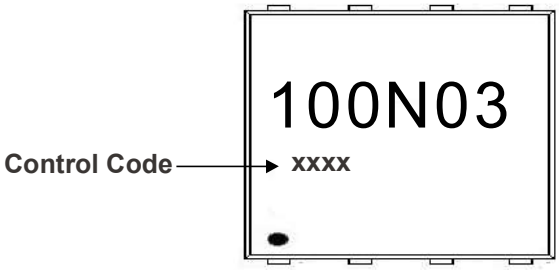
	SYMBOL	A	B	C	d	D	D1	D2
PDFN	(mm)	6.5 ± 0.10	5.30 ± 0.10	1.40 ± 0.10	1.50 ± 0.10	330 ± 1.00	178 ± 1.00	20.20 ± 1.00
	(inch)	0.256 ± 0.004	0.209 ± 0.004	0.055 ± 0.004	0.059 ± 0.004	13.00 ± 0.039	7.00 ± 0.039	0.795 ± 0.039

	SYMBOL	E	F	P	P0	P1	W	W1
PDFN	(mm)	1.75 ± 0.10	5.50 ± 0.10	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.10	12.00 + 1.00 / - 0.10	18.40 ± 1.00
	(inch)	0.069 ± 0.004	0.217 ± 0.004	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.004	0.472 + 0.039 / - 0.004	0.724 ± 0.039

Company reserves the right to improve product design , functions and reliability without notice.

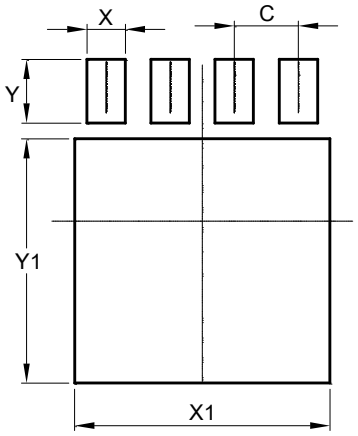
Marking Code

Part Number	Marking Code
CMS42N10H8	100N03



Suggested PAD Layout

Dimensions	Value (in mm)
C	1.270
X	0.610
X1	4.420
Y	1.270
Y1	4.520



Note:

1.The pad layout is for reference purposes only.

Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
PDFN	3,000	13