

CMS15P03Q8A-HF

P-Channel
RoHS Device
Halogen Free



Features

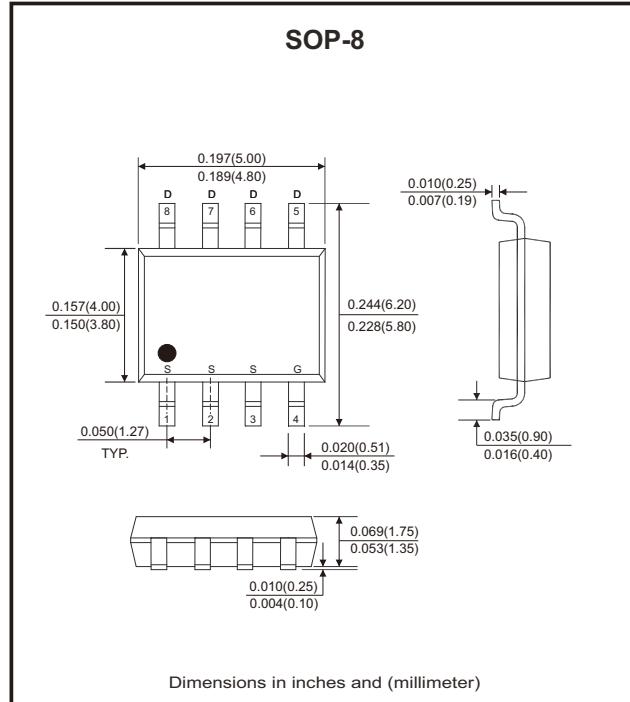
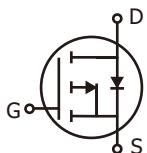
- Low on-resistance.
- Low Miller charge.
- Low input capacitance.
- Green device available.
- 100% EAS guaranteed.

Mechanical data

- Case: SOP-8 standard package, molded plastic.

Circuit Diagram

- G : Gate
- S : Source
- D : Drain



Maximum Ratings (at $T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	Value	Unit
Drain-source voltage		V_{DS}	-30	V
Gate-source voltage		V_{GS}	± 20	V
Continuous drain current (Note 1)	$I_D @ T_c = 25^\circ\text{C}$		-15	A
	$I_D @ T_c = 70^\circ\text{C}$		-12	
Pulsed drain current (Note 2)		I_{DM}	-31	A
Continuous drain current	$I_D @ T_a = 25^\circ\text{C}$		-8.6	A
	$I_D @ T_a = 70^\circ\text{C}$		-6.9	
Total power dissipation	$P_D @ T_c = 25^\circ\text{C}$		4.5	W
	$P_D @ T_a = 25^\circ\text{C}$		1.5	
Single pulse avalanche energy, $L=0.1\text{mH}$ (Note 3)		E_{AS}	105	mJ
Single pulse avalanche current, $L=0.1\text{mH}$ (Note 3)		I_{AS}	-46	A
Operating junction temperature range		T_J	-55 to +150	°C
Storage temperature range		T_{STG}	-55 to +150	°C
Thermal resistance junction-ambient (Note 2)	Steady state	$R_{\theta JA}$	85	°C/W
Thermal resistance junction-case (Note 2)	Steady state	$R_{\theta JC}$	28	°C/W

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Electrical Characteristics (at $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	BV_{DSS}	$V_{\text{GS}} = 0\text{V}, I_{\text{D}} = -250\mu\text{A}$	-30			V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = -250\mu\text{A}$	-1.0	-1.65	-2.5	
Forward transconductance	g_{fs}	$V_{\text{DS}} = -5\text{V}, I_{\text{D}} = -10\text{A}$		24		S
Gate-source leakage current	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$			± 100	nA
Drain-source leakage current ($T_J=25^\circ\text{C}$)	I_{DSS}	$V_{\text{DS}} = -24\text{V}, V_{\text{GS}} = 0\text{V}$			-1	μA
Static drain-source on-resistance (Note 2)	$R_{\text{DS(on)}}$	$V_{\text{GS}} = -10\text{V}, I_{\text{D}} = -12\text{A}$		10	12	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_{\text{D}} = -8\text{A}$		16	20	
Total gate charge (Note 2)	Q_g	$V_{\text{DS}} = -15\text{V}, I_{\text{D}} = -12\text{A}, V_{\text{GS}} = -4.5\text{V}$		21.5		nC
Gate-source charge	Q_{gs}			8.5		
Gate-drain ("miller") charge	Q_{gd}			7		
Turn-on delay time (Note 2)	$t_{\text{d(on)}}$	$V_{\text{DS}} = -15\text{V}, V_{\text{GS}} = -10\text{V}$ $I_{\text{D}} = -1\text{A}, R_{\text{G}} = 3.3\Omega$		7.84		nS
Rise time	t_r			72.2		
Turn-off delay time	$t_{\text{d(off)}}$			60.5		
Fall time	t_f			23.9		
Input capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -15\text{V}, f = 1\text{MHz}$		2129		pF
Output capacitance	C_{oss}			298		
Reverse transfer capacitance	C_{rss}			227		
Gate resistance	R_g	$f = 1\text{MHz}$		9		Ω
Source-drain diode						
Diode forward voltage	V_{SD}	$I_{\text{S}} = -1\text{A}, V_{\text{GS}} = 0\text{V}, T_J=25^\circ\text{C}$			-1.0	V
Continuous source current (Note 2,4)	I_s	$V_G = V_D = 0\text{V}$, Force current			-15	A
Pulsed source current (Note 2,4)	I_{SM}				-31	A
Reverse recovery time	t_{rr}	$I_F = -6\text{A}, T_J=25^\circ\text{C}$ $dI/dt = 100\text{A}/\mu\text{s}$		16.3		nS
Reverse recovery charge	Q_{rr}			5.9		nC
Guaranteed avalanche characteristics						
Single pulse avalanche energy (Note 3)	EAS	$V_{\text{DD}} = -25\text{V}, L=0.1\text{mH}, I_{\text{AS}} = -33\text{A}$	54			mJ

Notes: 1. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

2. R_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{JC} is guaranteed by design while R_{CA} is determined by the user's board design.
 R_{JA} shown below for single device operation on FR-4 in still air.

3. The min. value is 100% EAS tested guarantee.

4. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

Rating and Characteristic Curves (CMS15P03Q8A-HF)

Fig.1 - Typical Output Characteristics

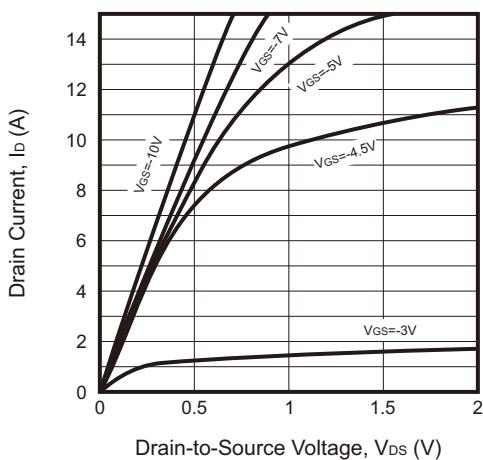


Fig.2 - On-Resistance vs. G-S Voltage

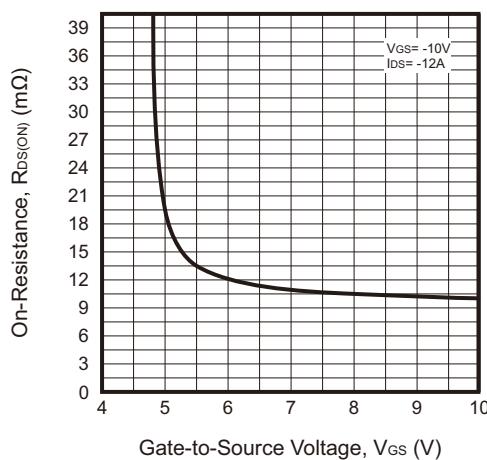


Fig.3 - On-Resistance vs. Drain Current

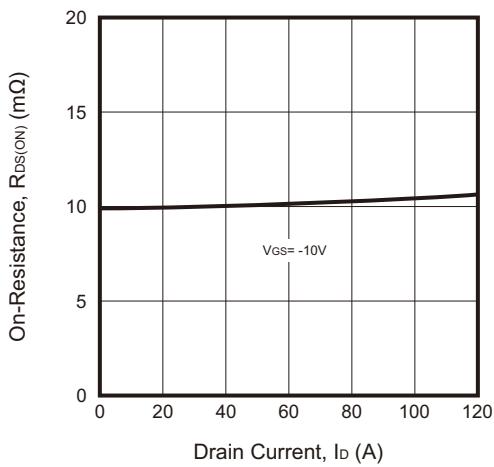


Fig.4 - Normalized $R_{DS(ON)}$ vs. T_J

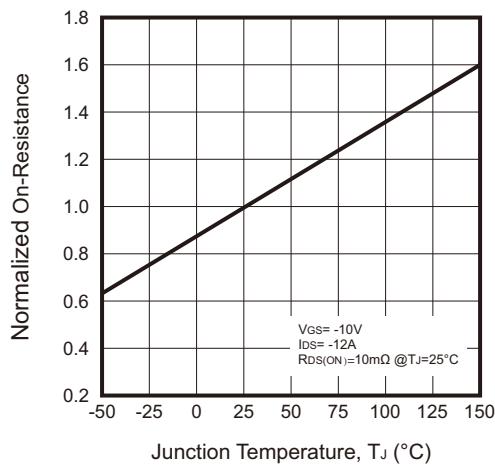


Fig.5 - Normalized $V_{GS(th)}$ vs. T_J

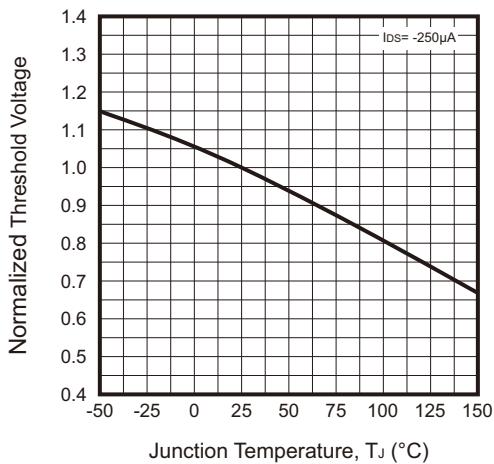
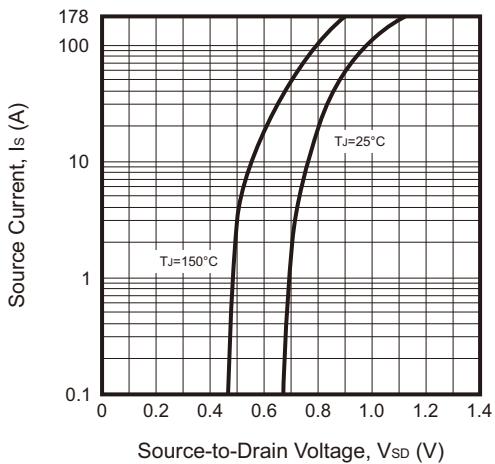


Fig.6 - Forward Characteristics of Reverse



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Rating and Characteristic Curves (CMS15P03Q8A-HF)

Fig.7 - Gate Charge Characteristics

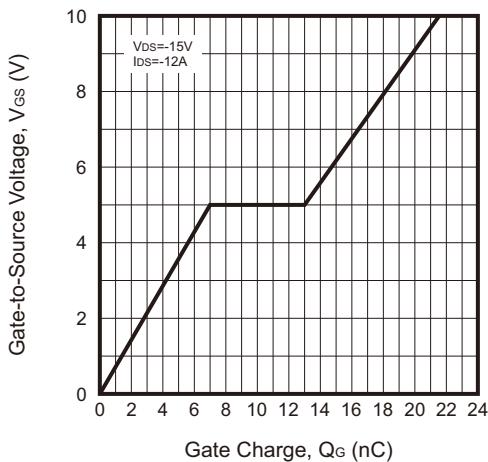


Fig.8 - Capacitance Characteristics

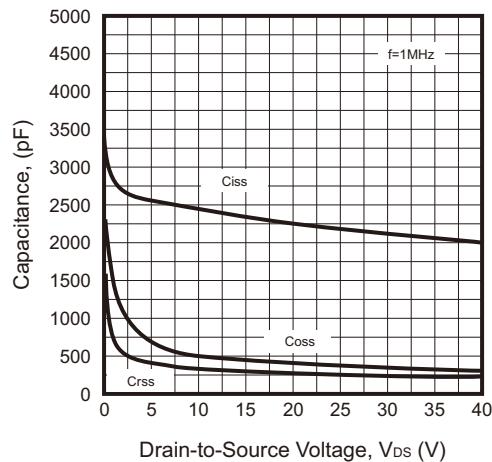


Fig.9 - Safe Operating Area

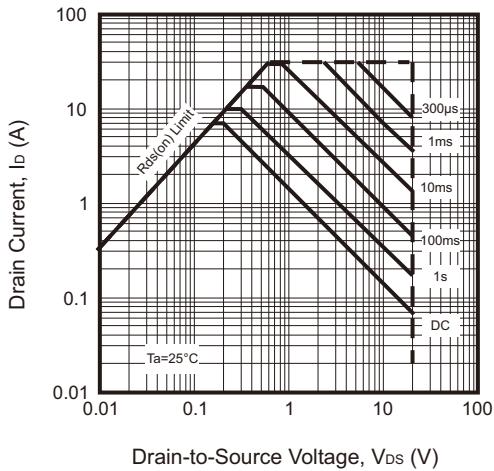


Fig.10 - Power Dissipation

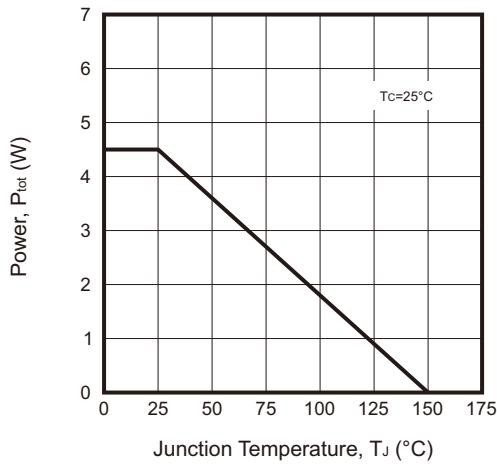
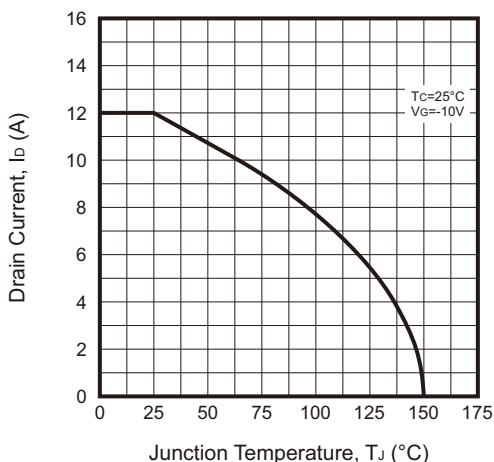


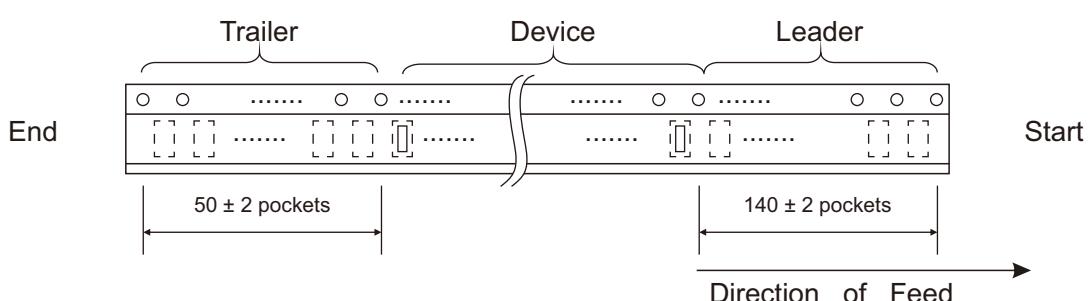
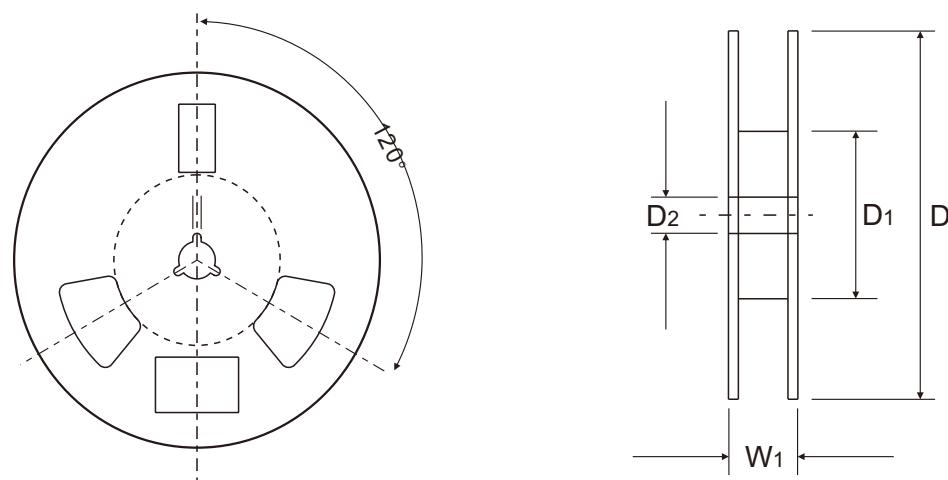
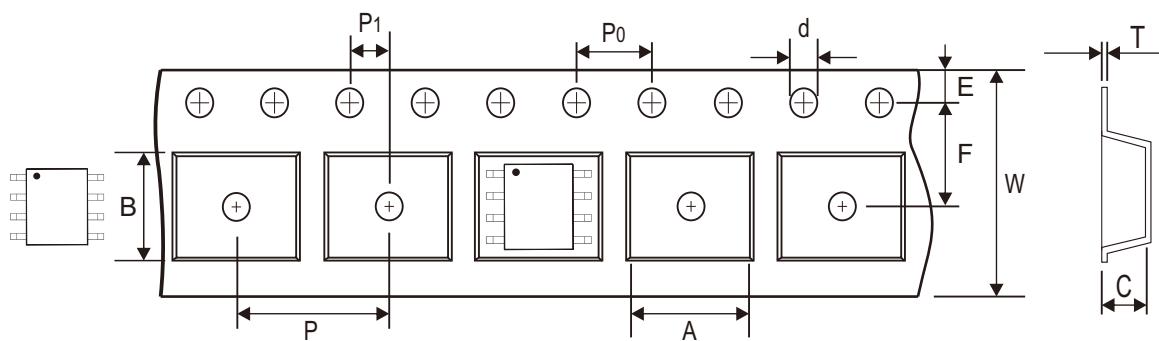
Fig.11 - Drain Current vs. T_J



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Reel Taping Specification



	SYMBOL	A	B	C	d	D	D1	D2
SOP-8	(mm)	6.50 ± 0.10	5.30 ± 0.10	2.10 ± 0.10	$1.50 + 0.10$ - 0.00	330.00 ± 1.00	$178.00 + 0.00$ - 2.00	13.00 min.
	(inch)	0.256 ± 0.004	0.209 ± 0.004	0.083 ± 0.004	$0.059 + 0.004$ - 0.000	12.992 ± 0.039	$7.008 + 0.000$ - 0.079	0.512 min.

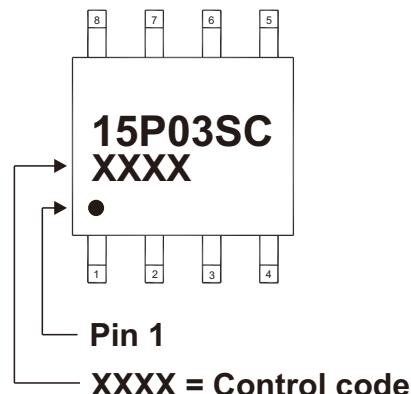
	SYMBOL	E	F	P	P ₀	P ₁	T	W	W ₁
SOP-8	(mm)	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.30 ± 0.05	12.00 ± 0.30	18.40 ref.
	(inch)	0.069 ± 0.004	0.217 ± 0.002	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.002	0.012 ± 0.002	0.472 ± 0.012	0.724 ref.

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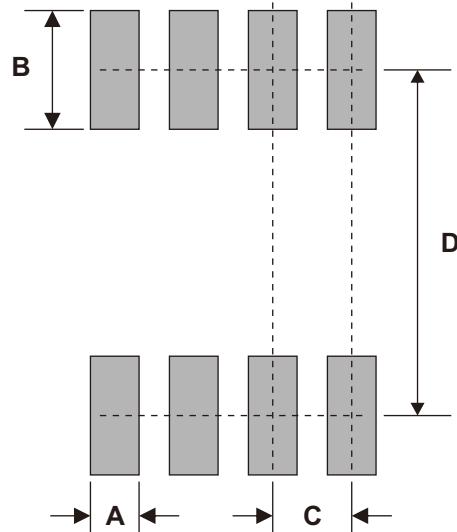
Marking Code

Part Number	Marking Code
CMS15P03Q8A-HF	15P03SC



Suggested PAD Layout

SIZE	SOP-8	
	(mm)	(inch)
A	0.65	0.026
B	1.75	0.069
C	1.27	0.050
D	5.60	0.220



Note: 1. The pad layout is for reference purposes only.

Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
SOP-8	3000	13