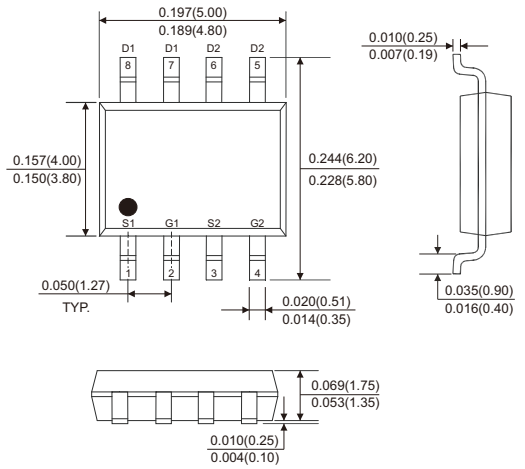
CMS06NP03Q8-HF

N and P-Channel
RoHS Device
Halogen Free

Features

- Advanced high cell density trench technology.
- Super low gate charge.
- Excellent cdv/dt effect decline.
- Green device available.
- 100% EAS guaranteed.

SOP-8



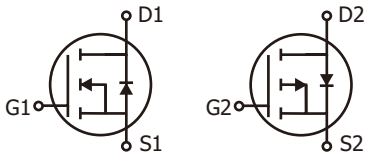
Dimensions in inches and (millimeter)

Mechanical data

- Case: SOP-8 standard package, molded plastic.

Circuit Diagram

- G : Gate
- S : Source
- D : Drain



Maximum Ratings (at Ta=25 °C unless otherwise noted)

Parameter	Conditions	Symbol	N-Channel	P-Channel	Unit
Drain-source voltage		V_{DS}	30	-30	V
Gate-source voltage		V_{GS}	±20	±20	V
Continuous drain current (Note 1)	I_D @ T_A = 25°C		6.9	-6.3	A
	I_D @ T_A = 70°C		5.5	-5.0	
Pulsed drain current (Note 2)		I_{DM}	20	-18	A
Total power dissipation (Note 4)	P_D @ T_A = 25°C		1.5		W
Single pulse avalanche energy, L=0.1mH (Note 3)		E_{AS}	22	45	mJ
Single pulse avalanche current, L=0.1mH (Note 3)		I_{AS}	21	-30	A
Operating junction temperature range		T_J	-55 to +150		°C
Storage temperature range		T_{STG}	-55 to +150		°C
Thermal resistance junction-ambient (Note 1)		$R_{\theta JA}$	83		°C/W
Thermal resistance junction-case (Note 1)		$R_{\theta JC}$	40		°C/W

N-Channel Electrical Characteristics (at T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	30			V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0		2.5	V
Forward transconductance	g_{fs}	V_{DS} = 5V, I_D = 7A		6		S
Gate-source leakage current	I_{GSS}	V_{GS} = ±20V			±100	nA
Drain-source leakage current (Tj=25°C)	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V			1	μA
Drain-source leakage current (Tj=55°C)		V_{DS} = 24V, V_{GS} = 0V			5	
Static drain-source on-resistance (Note 2)	$R_{DS(on)}$	V_{GS} = 10V, I_D = 6A			28	mΩ
		V_{GS} = 4.5V, I_D = 4A			42	
Total gate charge (Note 2)	Q_g	V_{DS} = 15V, I_D = 7A, V_{GS} = 4.5V		6		nC
Gate-source charge	Q_{gs}			2.5		
Gate-drain ("miller") charge	Q_{gd}			2.1		
Turn-on delay time (Note 2)	$t_{d(on)}$	V_{DS} = 15V, V_{GS} = 10V I_D = 7A, R_G = 3.3Ω		2.4		nS
Rise time	t_r			7.8		
Turn-off delay time	$t_{d(off)}$			22		
Fall time	t_f			4		
Input capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		572		pF
Output capacitance	C_{oss}			80		
Reverse transfer capacitance	C_{rss}			65		
Source-drain diode						
Diode forward voltage (Note 2)	V_{SD}	V_{GS} = 0V, I_S = 6A, T_J=25°C			1.2	V
Continuous source current (Note 1,6)	I_S	V_G = V_D = 0V, Force current			6.9	A
Pulsed source current (Note 2,6)	I_{SM}				20	A
Guaranteed avalanche characteristics						
Single pulse avalanche energy (Note 5)	EAS	V_{DD} = 25V, L=0.1mH, I_{AS} = 10A	5			mJ

Notes: 1. Surface mounted on a 1inch² FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width ≤300μs, duty cycle ≤ 2%.
3. The EAS data shows max. rating. The test condition is VDD=25V, VGS=10V, L=0.1mH, IAS=21A.
4. The power dissipation is limited by 150°C junction temperature.
5. The min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

P-Channel Electrical Characteristics (at T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-30			V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0		-2.5	V
Forward transconductance	g_{fs}	V_{DS} = -10V, I_D = -12A		13		S
Gate-source leakage current	I_{GSS}	V_{GS} = ±20V			±100	nA
Drain-source leakage current (Tj=25°C)	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
Drain-source leakage current (Tj=55°C)		V_{DS} = -24V, V_{GS} = 0V			-5	
Static drain-source on-resistance (Note 2)	$R_{DS(on)}$	V_{GS} = -10V, I_D = -6A			36	mΩ
		V_{GS} = -4.5V, I_D = -4A			55	
Total gate charge (Note 2)	Q_g	V_{DS} = -20V, I_D = -12A, V_{GS} = -4.5V		9.8		nC
Gate-source charge	Q_{gs}			2.2		
Gate-drain ("miller") charge	Q_{gd}			3.4		
Turn-on delay time (Note 2)	$t_{d(on)}$	V_{DS} = -24V, V_{GS} = -10V I_D = -1A, R_G = 3.3Ω		16.4		nS
Rise time	t_r			20.2		
Turn-off delay time	$t_{d(off)}$			55		
Fall time	t_f			10		
Input capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		930		pF
Output capacitance	C_{oss}			148		
Reverse transfer capacitance	C_{rss}			115		
Source-drain diode						
Diode forward voltage (Note 2)	V_{SD}	V_{GS} = 0V, I_S = -6A, T_J=25°C			-1.2	V
Continuous source current (Note 1,6)	I_S	V_G = V_D = 0V, Force current			-6.3	A
Pulsed source current (Note 2,6)	I_{SM}				-18	A
Guaranteed avalanche characteristics						
Single pulse avalanche energy (Note 5)	EAS	V_{DD} = -25V, L=0.1mH, I_{AS} = -10A	5			mJ

Notes: 1. Surface mounted on a 1inch² FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width ≤300μs, duty cycle ≤ 2%.
3. The EAS data shows max. rating. The test condition is VDD=-25V, VGS=-10V, L=0.1mH, IAS=-30A.
4. The power dissipation is limited by 150°C junction temperature.
5. The min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

N-Channel Rating and Characteristic Curves (CMS06NP03Q8-HF)

Fig.1 - Typical Output Characteristics

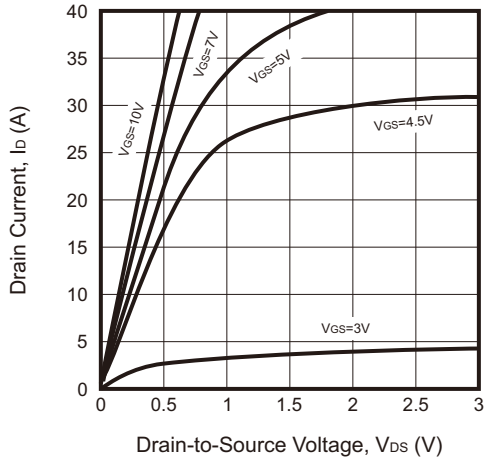


Fig.2 - On-Resistance vs. G-S Voltage

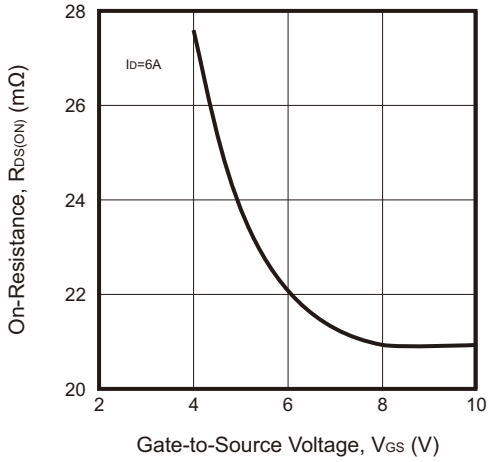


Fig.3 - Normalized $V_{GS(th)}$ vs. T_J

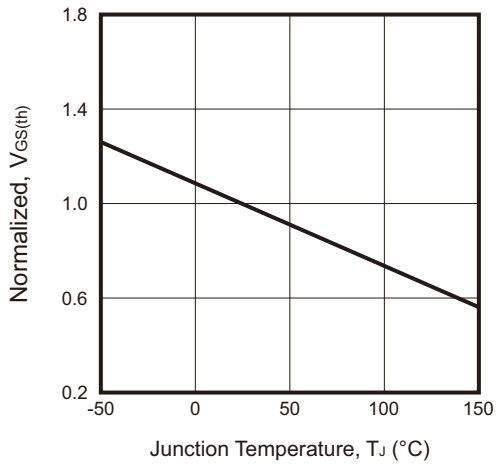


Fig.4 - Normalized $R_{DS(ON)}$ vs. T_J

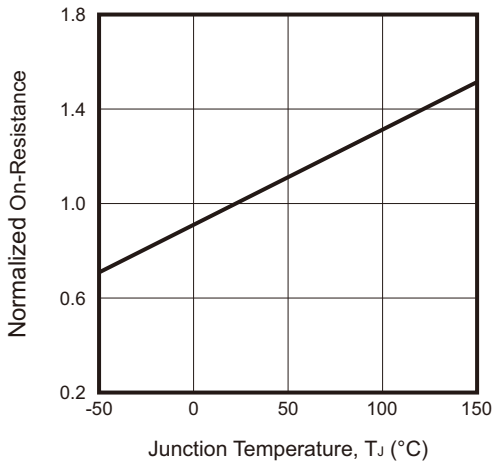


Fig.5 - Safe Operating Area

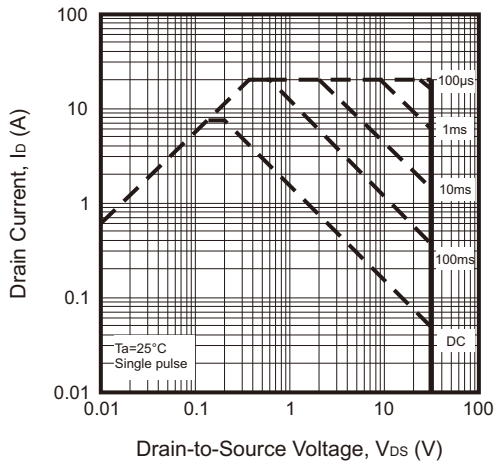
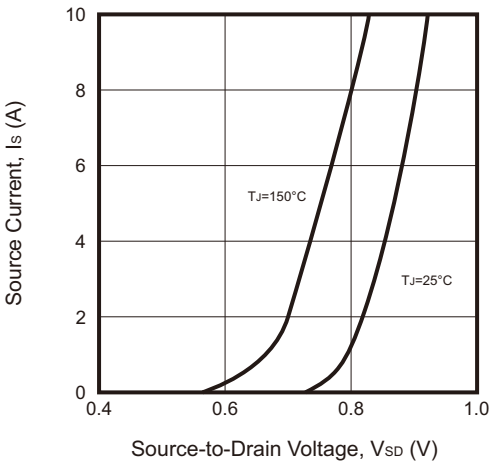


Fig.6 - Forward Characteristics of Reverse



N-Channel Rating and Characteristic Curves (CMS06NP03Q8-HF)

Fig.7 - Gate Charge Characteristics

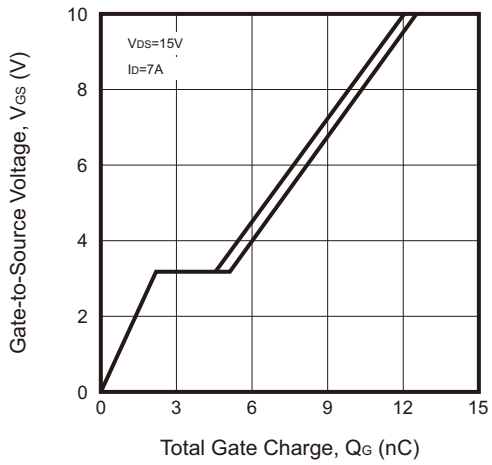
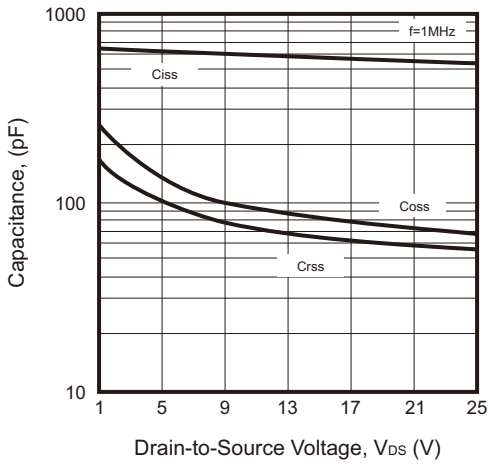


Fig.8 - Capacitance Characteristics



P-Channel Rating and Characteristic Curves (CMS06NP03Q8-HF)

Fig.1 - Typical Output Characteristics

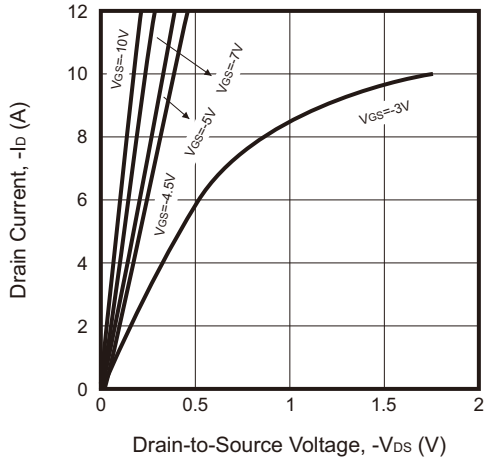


Fig.2 - On-Resistance vs. G-S Voltage

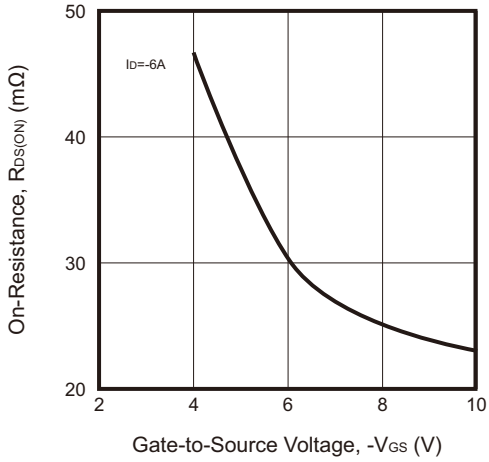


Fig.3 - Normalized $V_{GS(th)}$ vs. T_J

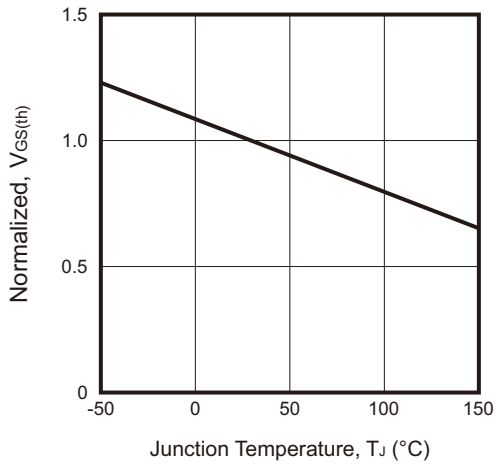


Fig.4 - Normalized $R_{DS(ON)}$ vs. T_J

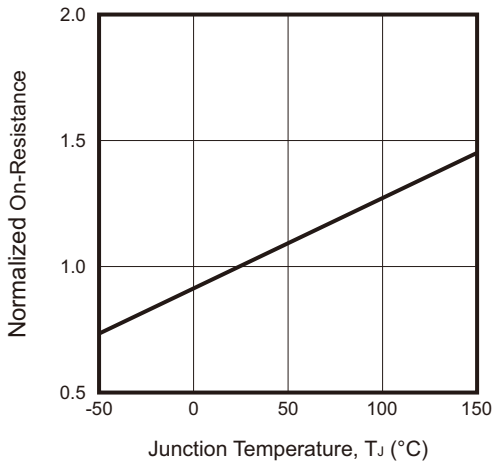


Fig.5 - Safe Operating Area

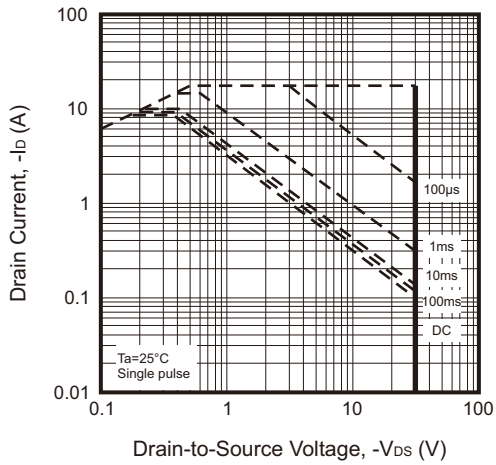
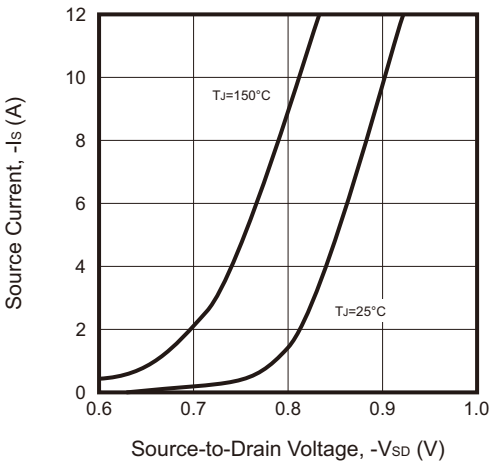


Fig.6 - Forward Characteristics of Reverse



P-Channel Rating and Characteristic Curves (CMS06NP03Q8-HF)

Fig.7 - Gate Charge Characteristics

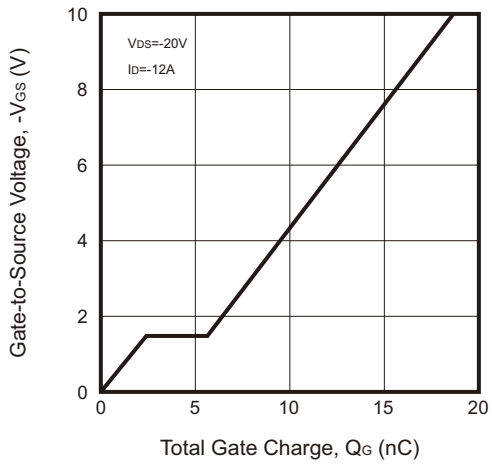
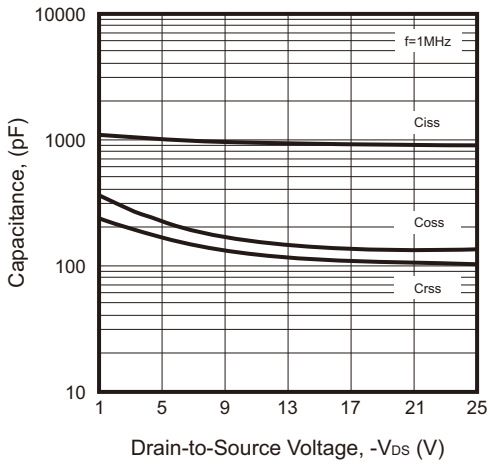
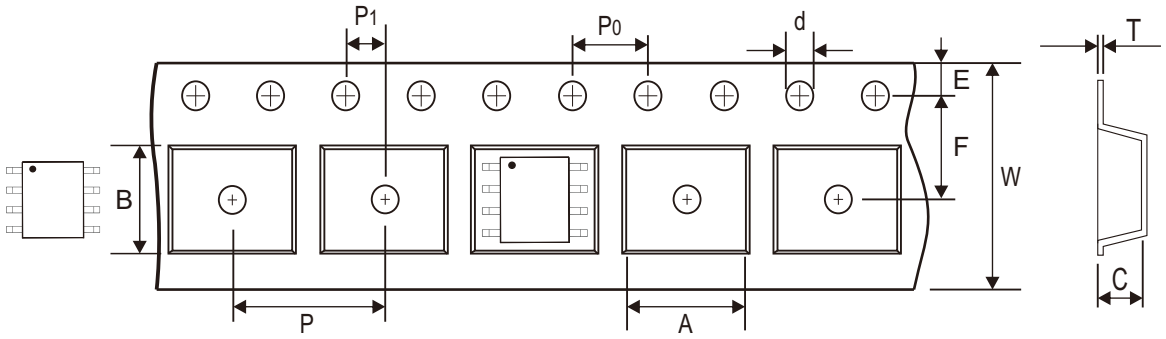
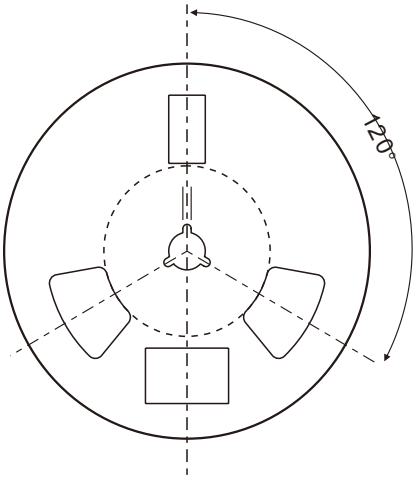


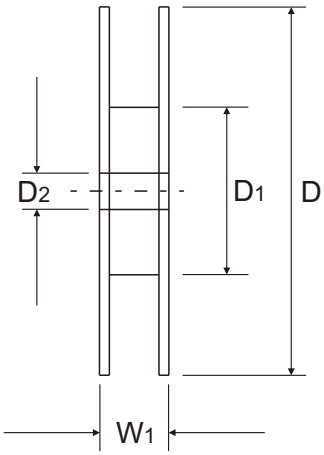
Fig.8 - Capacitance Characteristics

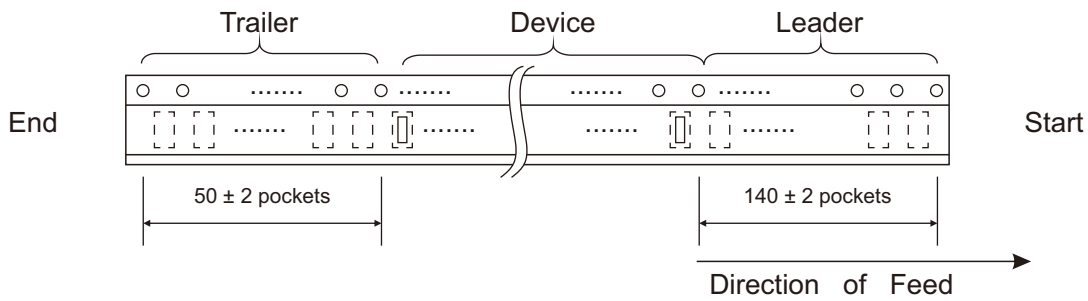


Reel Taping Specification







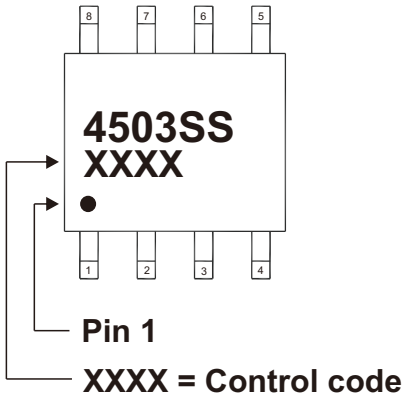


	SYMBOL	A	B	C	d	D	D1	D2
SOP-8	(mm)	6.50 ± 0.10	5.30 ± 0.10	2.10 ± 0.10	1.50 + 0.10 - 0.00	330.00 ± 1.00	178.00 + 0.00 - 2.00	13.00 min.
	(inch)	0.256 ± 0.004	0.209 ± 0.004	0.083 ± 0.004	0.059 + 0.004 - 0.000	12.992 ± 0.039	7.008 + 0.000 - 0.079	0.512 min.

	SYMBOL	E	F	P	P0	P1	T	W	W1
SOP-8	(mm)	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.30 ± 0.05	12.00 ± 0.30	18.40 ref.
	(inch)	0.069 ± 0.004	0.217 ± 0.002	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.002	0.012 ± 0.002	0.472 ± 0.012	0.724 ref.

Marking Code

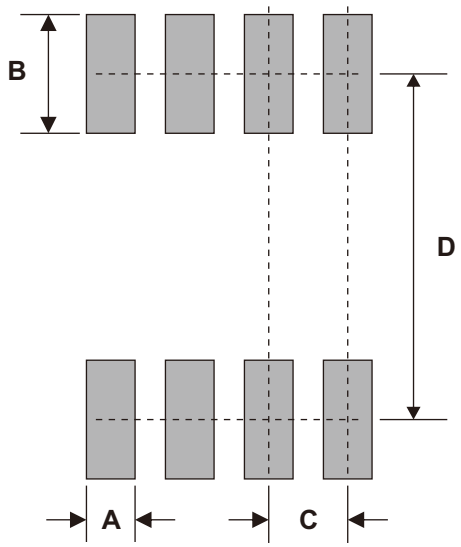
Part Number	Marking Code
CMS06NP03Q8-HF	4503SS



Suggested PAD Layout

SIZE	SOP-8	
	(mm)	(inch)
A	0.65	0.026
B	1.75	0.069
C	1.27	0.050
D	5.60	0.220

Note: 1. The pad layout is for reference purposes only.



Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
SOP-8	3000	13