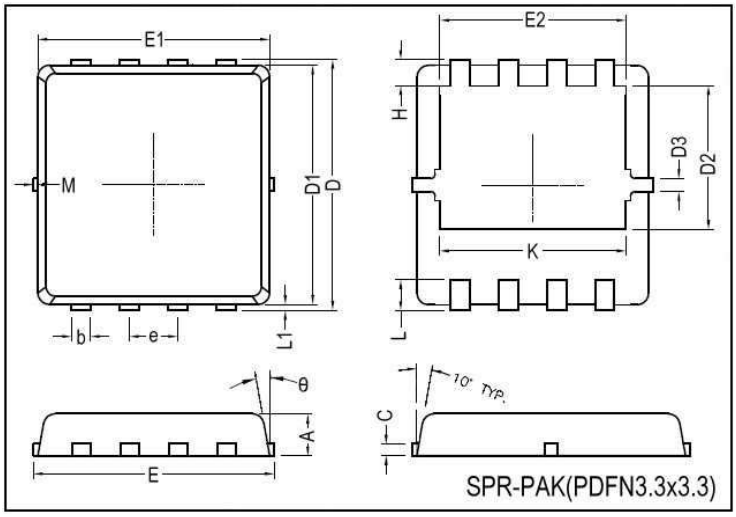
CMS30N10V8-HF

N-Channel
RoHS Device
Halogen Free



Description

The CMS30N10V8 uses advanced Trench technology and designs to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

The CMS30N10V8 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

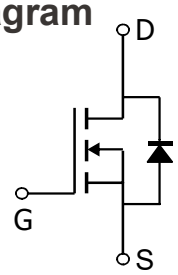
Features

-Low On-Resistance
-Low Input Capacitance
-Green Device Available
-Low Miller Charge
-100% EAS Guaranteed

REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.70	0.75	0.80	E1	3.00	3.15	3.20
b	0.25	0.30	0.35	E2	2.39	2.49	2.59
C	0.10	0.15	0.25	e	0.65 BSC		
D	3.25	3.35	3.45	H	0.30	0.39	0.50
D1	3.00	3.10	3.20	L	0.30	0.40	0.50
D2	1.48	1.58	1.68	L1	-	0.13	0.20
D3	-	0.13	-	θ	-	10°	12°
E	3.20	3.30	3.40	M	-	-	0.15

Circuit diagram

- G : Gate
- S : Source
- D : Drain



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D @T_C=25℃	30	A
	I_D @T_C=70℃	24	A
Pulsed Drain Current[1]	I_{DM}	50	A
Continuous Drain Current	I_D @T_A=25℃	7.8	A
	I_D @T_A=70℃	6.3	A
Total Power Dissipation	P_D @T_C=25℃	31.3	W
	P_D @T_A=25℃	2.1	W
Single Pulse Avalanche Energy, L=3mH	E_{AS}	63	mJ
Single Pulse Avalanche Current, L=3mH	I_{AS}	6.5	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	℃

Thermal Data

Parameter	Symbol	Conditions	Max. Value	Unit
Thermal Resistance Junction-ambient[2]	$R_{\theta JA}$	Steady State	60	℃/W
Thermal Resistance Junction-case[2]	$R_{\theta JC}$	Steady State	4	℃/W

Electrical Characteristics (Tj = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	100	-	-	V	V_{GS}=0, I_D=250uA
Gate Threshold Voltage	$V_{GS(th)}$	1.2	1.8	2.5	V	V_{DS}=V_{GS}, I_D=250uA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	I_{DSS}	-	-	1	uA	V_{DS}=80V, V_{GS}=0
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	20	24	mΩ	V_{GS}=10V, I_D=10A
		-	22	28		V_{GS}=4.5V, I_D=10A
Total Gate Charge	Q_g	-	34	-	nC	I_D=10A V_{DS}=50V V_{GS}=10V
Gate-Source Charge	Q_{gs}	-	6	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	9	-		
Turn-on Delay Time	$T_{d(on)}$	-	7	-	ns	V_{DS}=50V V_{GS}=10V R_G=3Ω R_L=5Ω
Rise Time	T_r	-	7	-		
Turn-off Delay Time	$T_{d(off)}$	-	29	-		
Fall Time	T_f	-	7	-		
Input Capacitance	C_{iss}	-	1325	-	pF	V_{GS}=0V V_{DS}=30V f=1.0MHz
Output Capacitance	C_{oss}	-	110	-		
Reverse Transfer Capacitance	C_{rss}	-	64	-		

Guaranteed Avalanche Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy[3]	EAS	34.5	-	-	mJ	V_{DD}=50V, L=3mH, I_{AS}=4.8A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Diode Forward Voltage	V_{SD}	-	-	1.3	V	I_S=10A, V_{GS}=0V
Reverse Recovery Time	t_{rr}	-	32	-	ns	I_F=10A, dI/dt=500A/μs, T_J=25℃
Reverse Recovery Charge	Q_{rr}		200	-	nC	

Notes: 1. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.

3. The Min. value is 100% EAS tested guarantee.

TYPICAL CHARACTERISTIC

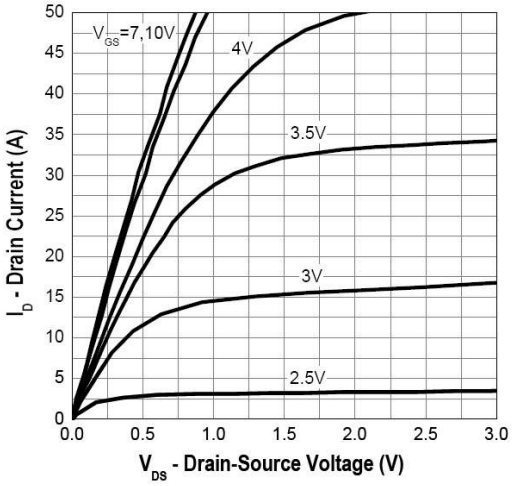


Fig.1 Typical Output Characteristics

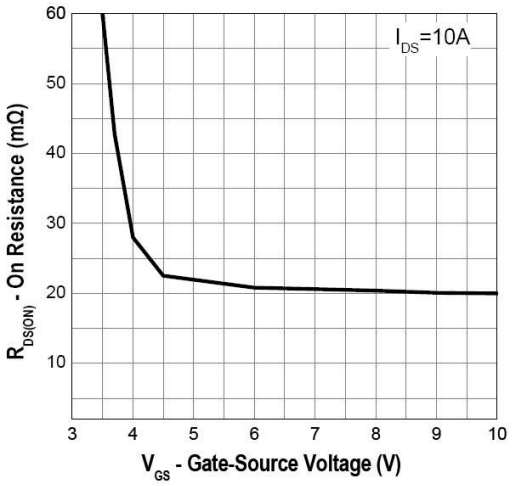


Fig.2 On-Resistance vs. G-S Voltage

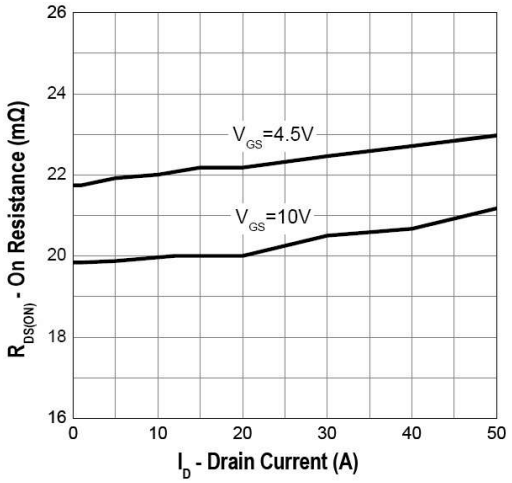


Fig.3 On-Resistance vs. Drain Current

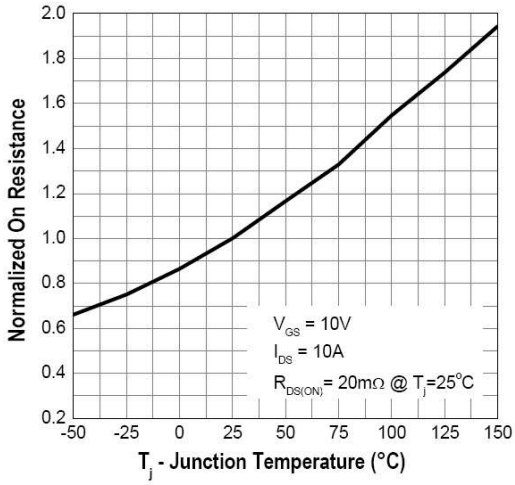


Fig.4 Normalized R_{DSON} vs. T_J

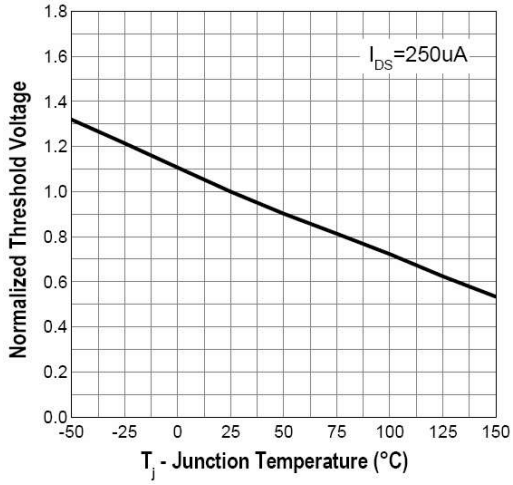


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

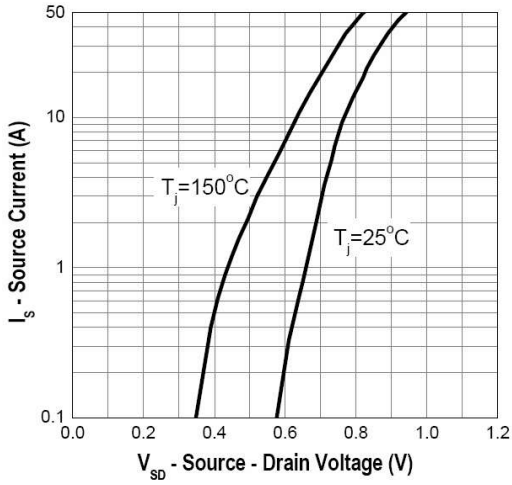


Fig.6 Forward Characteristics of Reverse

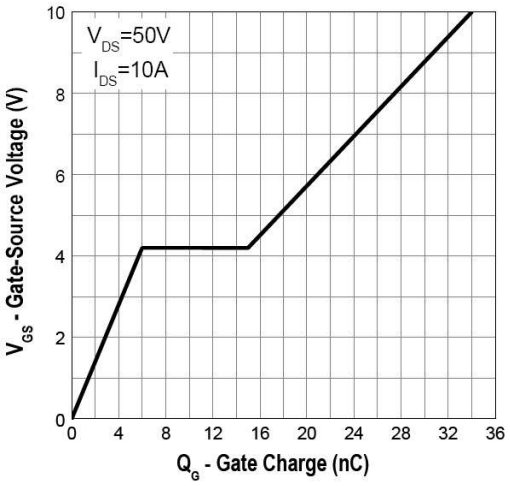


Fig.7 Gate Charge Characteristics

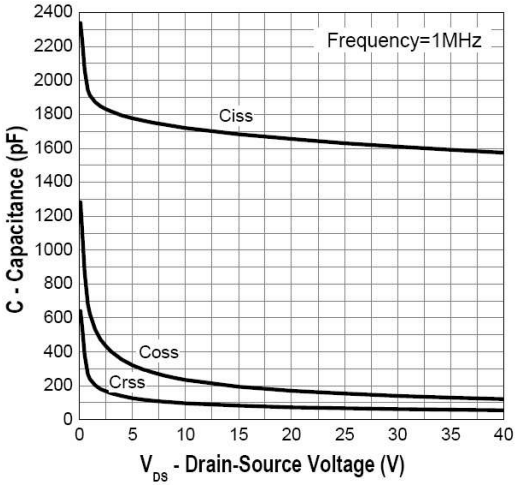


Fig.8 Capacitance Characteristic

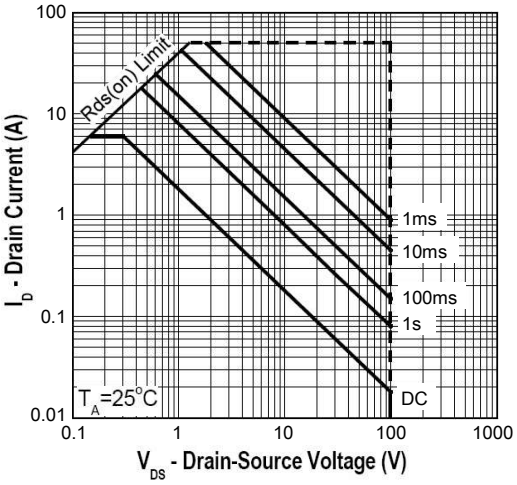


Fig.9 Safe Operating Area

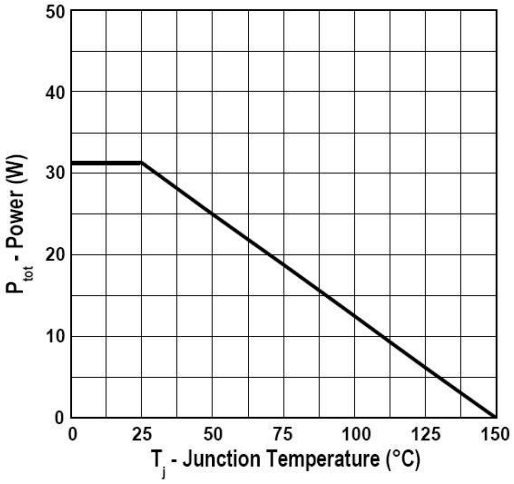


Fig.10 Power Dissipation

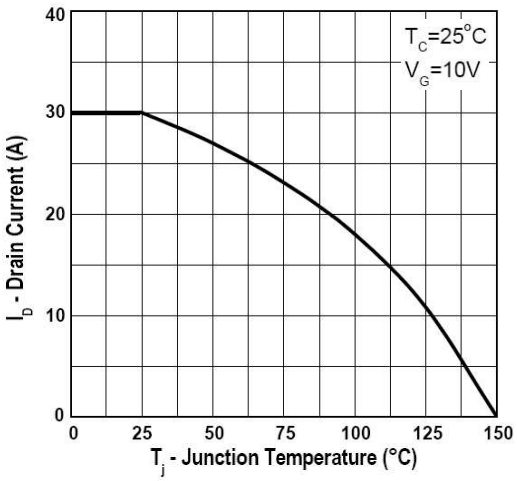


Fig.11 Drain Current vs. T_J

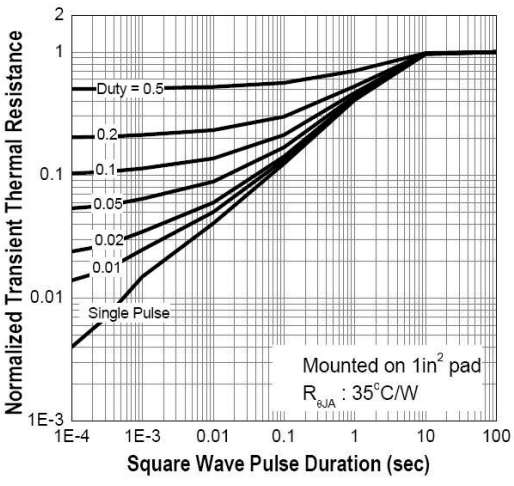
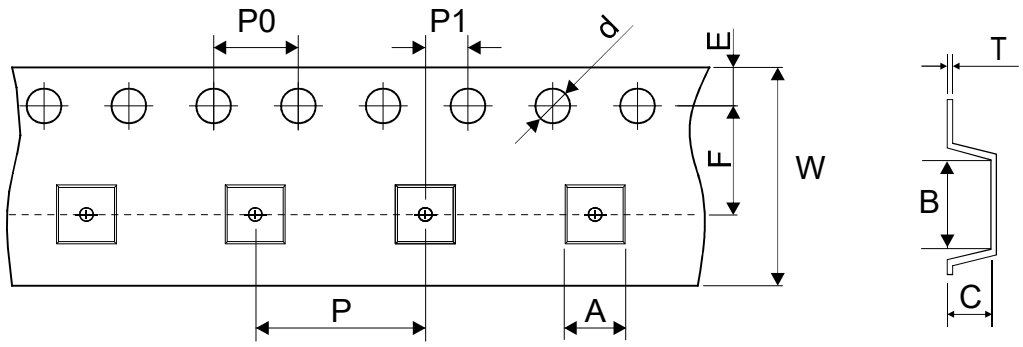
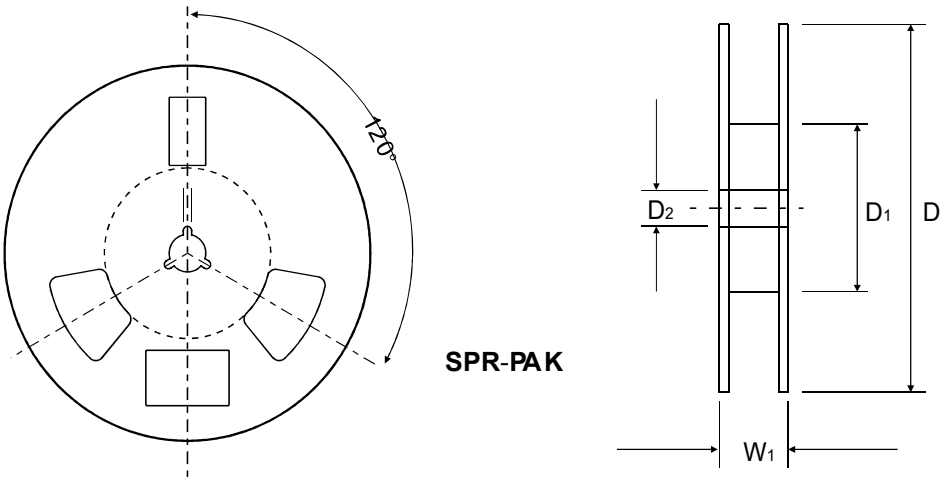


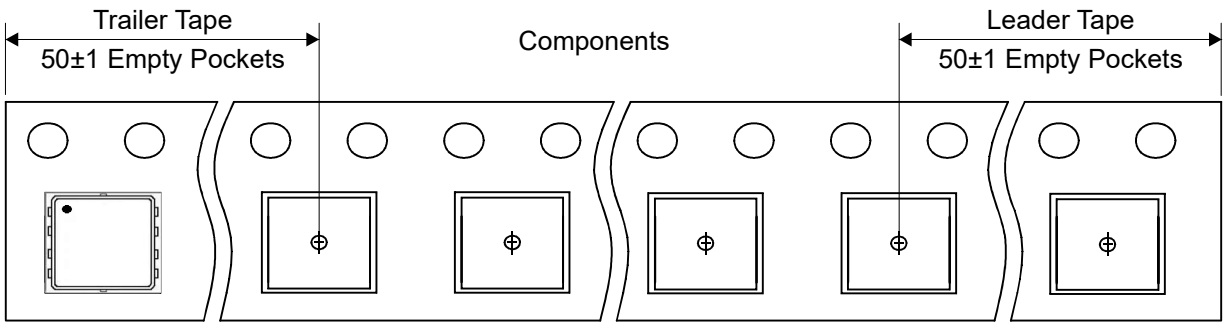
Fig.12 Transient Thermal Impedance

Reel Taping Specification





SPR-PAK



	SYMBOL	A	B	C	d	D	D1	D2
SPR-PAK	(mm)	3.55 ± 0.10	3.55 ± 0.10	1.40 ± 0.10	1.50 ± 0.10	330 ± 1.00	178 ± 1.00	20.20 ± 1.00
	(inch)	0.139 ± 0.004	0.139 ± 0.004	0.055 ± 0.004	0.059 ± 0.004	13.00 ± 0.039	7.00 ± 0.039	0.795 ± 0.039

	SYMBOL	E	F	P	P0	P1	W	W1
SPR-PAK	(mm)	1.75 ± 0.10	5.50 ± 0.10	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.10	12.00 + 1.00 / - 0.10	18.40 ± 1.00
	(inch)	0.069 ± 0.004	0.217 ± 0.004	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.004	0.472 + 0.039 / - 0.004	0.724 ± 0.039

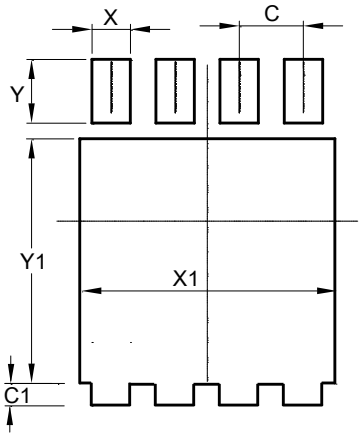
Company reserves the right to improve product design , functions and reliability without notice.

Marking Code

Part Number	Marking Code
CMS30N10V8-HF	100N03

Suggested PAD Layout

Dimensions	Value (in mm)
C	0.65
C1	0.40
X	0.40
X1	2.80
Y	0.60
Y1	2.35



Note:

1.The pad layout is for reference purposes only.

Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
PDFN	3,000	13