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Low Clamping Voltage CPDVR083V3UA
Product Application Notes

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By: Ken Liang
Address: No.31, Yong Hsin Lane, Yingtau Rd,
Yingge Town, Taipei County, Taiwan
TEL: 886-2-86776675

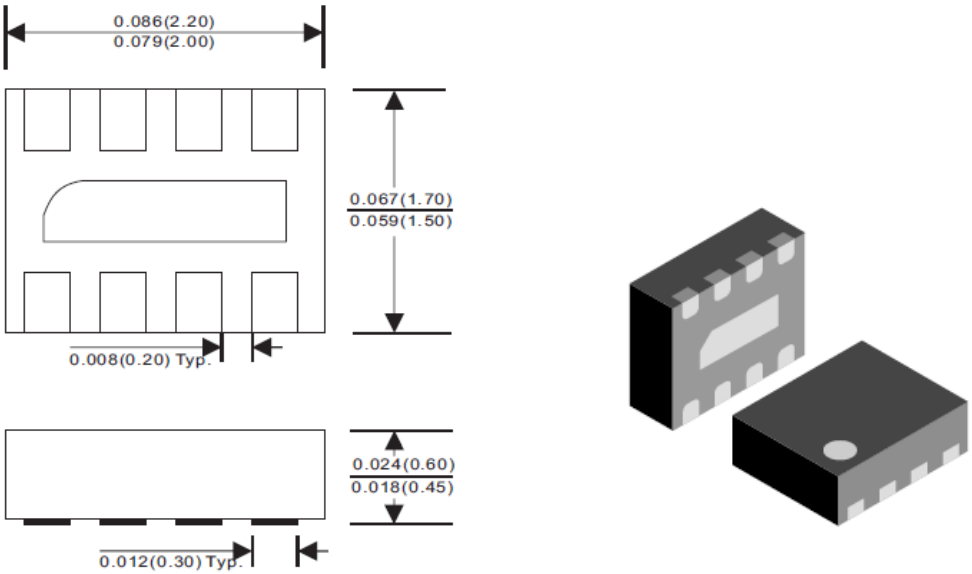
Products Description

ESD Protection Array—3.3V Multi-Line

The CPDVR083V3UA is a 3.3V 4-line ESD protection array that meets the immunity requirements of IEC 61000-4-2 level 4(±15KV air,±8KV contact discharge).It features a flow through design that simplifies layout and reduces board space required by 4 single-line discrete devices.

The layout required for the device results in improve ESD performance due to reduced board trace inductance. The result is lower clamping voltage and a higher level of protection when compared to conventional ESD devices.

The CPDVR083V3UA is a 8-pin package measuring 2.2 x 1.7 x 0.6mm. The flat-chip, SOT-383F package is RoHS, Halogen-Free, and Tin-Free, making it ideal for use in portable electronics such as cell phone, digital camera and PND.



Package

Features

Halogen free
IEC6100-4-2(ESD)±15KV(contact), ±20KV(air)
Working voltage 3.3V
Protects four I/O line
Flow through design for easy layout
Small package retrench board space
Low leakage current
Low operating and clamping voltages

Applications

Portable handheld devices
Notebook
Portable GPS
Digital Camera
MP3 Players

Specifications

Maximum Rating (at T_A=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak pulse power(tp=8/20 us)	Ppp	40	W
Peak pulse current(tp=8/20 us)	Ipp	5	A
ESD per IEC 61000-4-2(Air) ESD per IEC 61000-4-2(Contact)	ESD	±20 ±15	kV
Operating Temperature	TJ	-55 to +125	℃
Storage Temperature	TSTG	-55 to +125	℃

Electrical Characteristics (at T_A=25℃ unless otherwise noted)

Parameter	Conditions	Symbol	Typ	Max	Unit
Reverse stand-off voltage		V_{RWM}		3.3	V
Leakage current	VR=3.3V	I_L	0.05	0.5	uA
Clamping voltage	Ipp=1A, Tp=8/20us, Any channel pin to ground	V_C		5.5	V
	Ipp=5A,Tp=8/20us, Any channel pin to ground	V_C		8.0	V
Reverse clamping voltage	Ipp=5A,Tp=8/20us	V_{CR}		2.4	V
Junction capacitance	VR=0V,f=1MHz Any channel pin to ground	C_j	25	30	pF
	VR=3.3V,f=1MHz Any channel pin to ground	C_j	14		pF

Typical Characteristics

Fig. 1 - Non-repetitive max. peak pulse power vs. pulse time

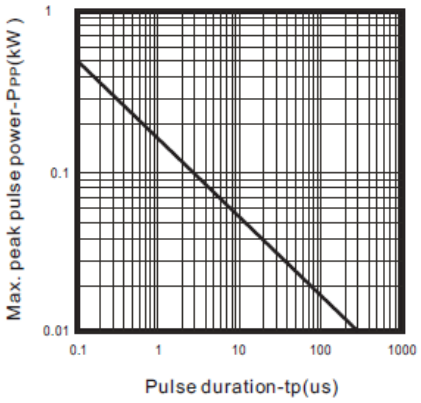


Fig. 2 - Power rating derating curve

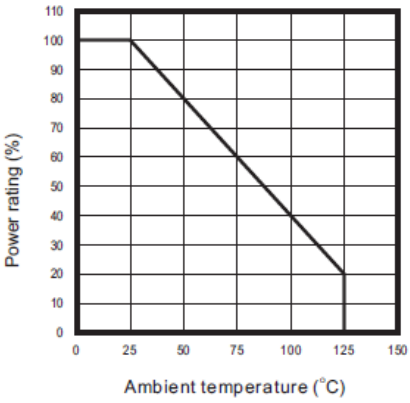


Fig.3 - Clamping voltage vs. peak pulse current

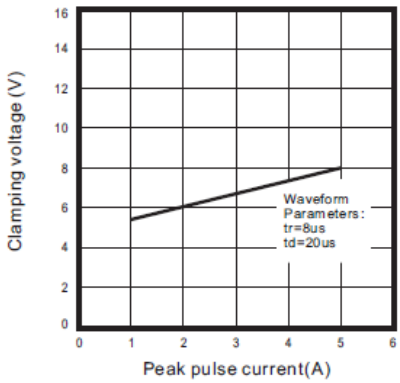


Fig.4 - Forward voltage vs. Forward current

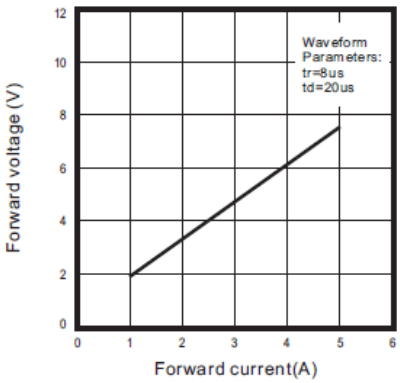
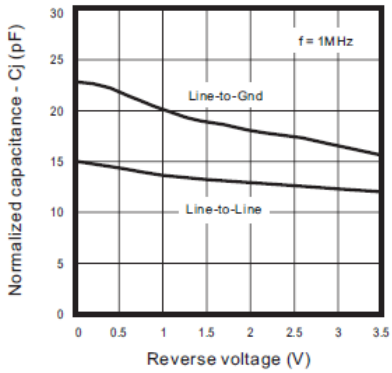


Fig.5 - Junction capacitance vs. reverse voltage



Applications Information

The CPDVR083V3UA is designed to protect four line against system. Under normal circumstance will present high impedance to protected line up to 3.3V. When the line voltage exceeds 3.5V will turn on.

The easy for PCB layout by allowing the traces to enter one side of the device and exit the other side. The recommended way to design the PCB board traces in order to use the flow through layout.

The output pin is opposite to input pin (pin1 to pin8, pin2 to pin7, pin3 to pin6, pin4 to pin5). The bottom tab is connected to ground. This connection should be made directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance.

The using CPDVR083V3UA protect the data line and control line reduces required board space by as much as 70% over 0402 size discrete solutions.

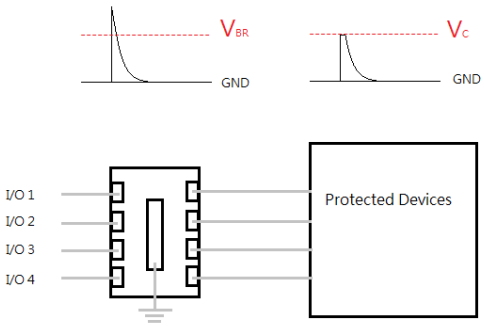


Figure.1

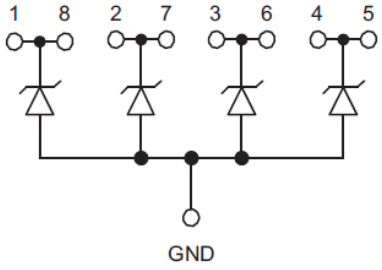


Figure.2

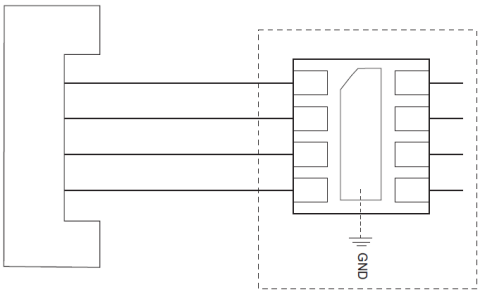


Figure.3

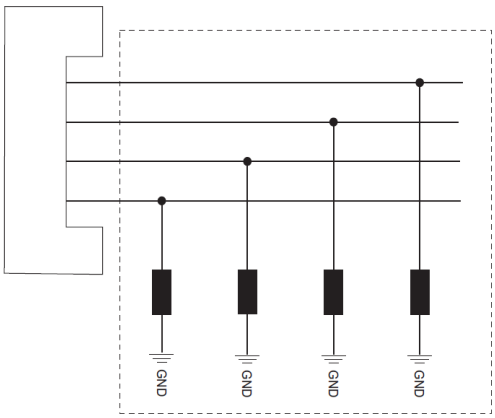


Figure4