SMD Diodes Specialist

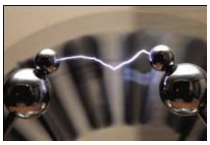
Comchip Technology Corporation

ESD Protection Diode
CPDVR083V3UA-HF (SOT-383F Package)
New Product Announcement

Issued: 2010/09/01
Version: CM001-A
By: Ken Liang
Address: No.31, Yong Hsin Lane, Yingtau Rd,
Yingge Town, Taipei County, Taiwan
TEL: 886-2-86776675

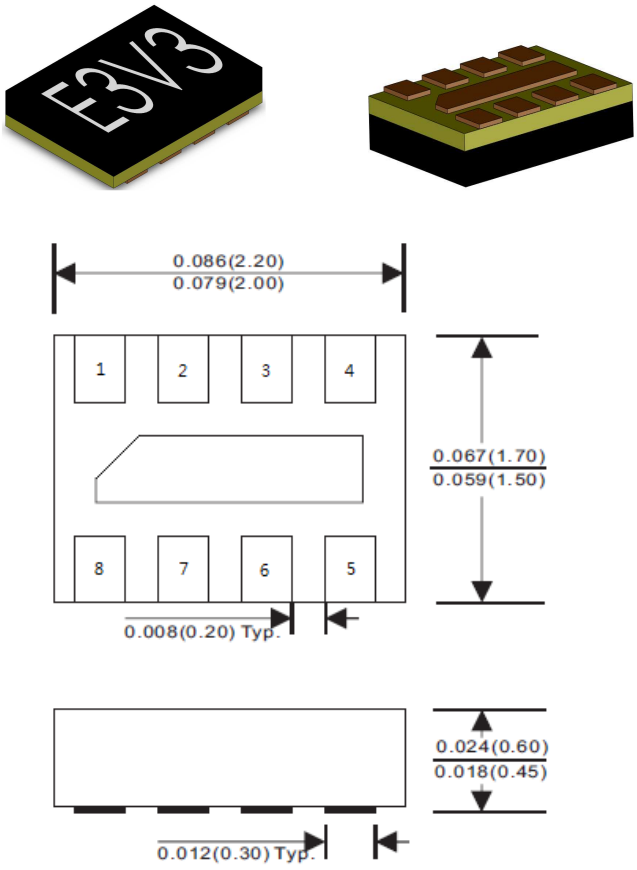
Product Description

ESD Protection Array—3.3V Multi-Line



Comchip's CPDVR083V3UA-HF is a 3.3V unidirectional 4-line ESD protection array diode that meets the immunity requirements of IEC 61000-4-2 level 4 (± 20kV air, ±15kV contact discharge). It features a flow through design that simplifies board layout and reduces board space when compared to 4 single-line discrete devices. This device improves ESD performance by reducing board trace inductance which results in a lower clamping voltage and a higher level of protection when compared to conventional ESD devices.

The CPDVR083V3UA-HF utilizes the 8-pin SOT-383F flat chip package which measures: 2.100 x 1.600 x 0.525mm. The device has gold terminations and is RoHS compliant and completely Tin-Free. This small package makes it ideal for uses in portable electronics such as cell phones, digital cameras, and personal navigation devices.



Package

Features

Halogen free
IEC6100-4-2(ESD) ±15kV(contact), ±20kV(air)
Working voltage: 3.3V
Protects four I/O lines
Flow through design for easy board layout
Small package retrenches board space
Low leakage currents
Low operating and clamping voltages

Applications

Portable handheld devices
Portable GPS devices
MP3 Players
Notebooks
Digital Cameras

Specifications

Maximum Rating (at T_A=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Peak pulse power(tp=8/20 us)	Ppp	40	W
Peak pulse current(tp=8/20 us)	Ipp	5	A
ESD per IEC 61000-4-2(Air) ESD per IEC 61000-4-2(Contact)	ESD	±20 ±15	kV
Operating Temperature	TJ	-55 to +125	°C
Storage Temperature	TSTG	-55 to +125	°C

Electrical Characteristics (at T_A=25°C unless otherwise noted)

Parameter	Conditions	Symbol	Typ	Max	Unit
Reverse stand-off voltage		V_{RWM}		3.3	V
Leakage current	VR=3.3V	I_L	0.05	0.5	uA
Clamping voltage	Ipp=1A, Tp=8/20us, Any channel pin to ground	V_C		5.5	V
	Ipp=5A,Tp=8/20us, Any channel pin to ground	V_C		8.0	V
Reverse clamping voltage	Ipp=5A,Tp=8/20us	V_{CR}		2.4	V
Junction capacitance	VR=0V,f=1MHz Any channel pin to ground	C_j	25	30	pF
	VR=3.3V,f=1MHz Any channel pin to ground	C_j	14		pF

Typical Characteristics

Fig. 1 - Non-repetitive max. peak pulse power vs. pulse time

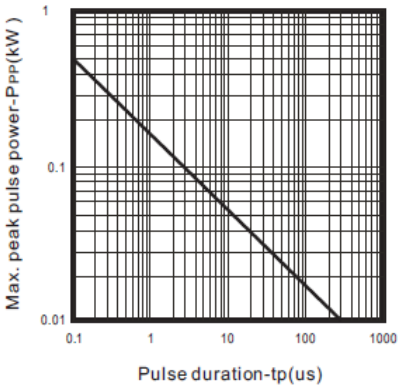


Fig. 2 - Power rating derating curve

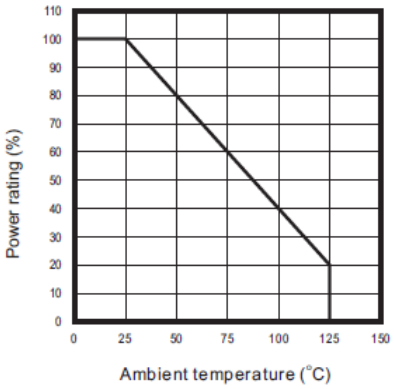


Fig.3 - Clamping voltage vs. peak pulse current

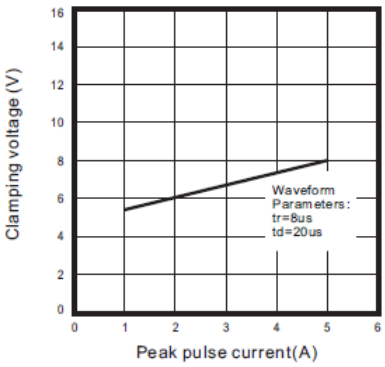


Fig.4 - Forward voltage vs. Forward current

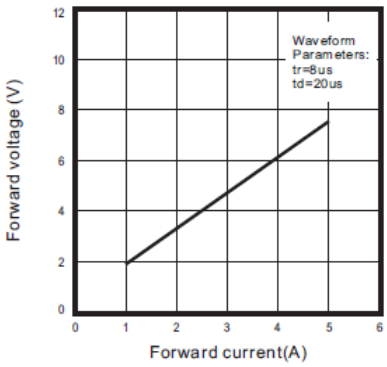
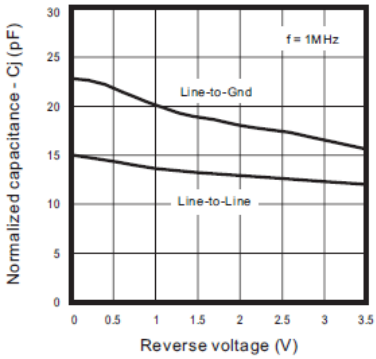


Fig.5 - Junction capacitance vs. reverse voltage



Application Information

The CPDVR083V3UA-HF is designed to protect four lines against surge conditions. Under normal circumstances, the CPDVR083V3UA-HF will present high impedances to protected lines up to 3.3V. When the line voltage exceeds the trigger voltage of 3.5V the diode will activate.

The CPDVR083V3UA-HF is ideal for easy PCB layout by allowing the traces to enter one side of the device and exit the other. The recommended design for PCB board traces is to use the flow through layout.

The output pins are opposite to the input pins (pin1 to pin8, pin2 to pin7, pin3 to pin6, pin4 to pin5). The bottom pin is grounded. This connection should be made directly to a grounded plane on the board for best results. Keep the path length as short as possible to minimize parasitic inductance.

The size of the SOT-383F thin chip package reduces required board space by as much as 70% over individual discrete solutions.

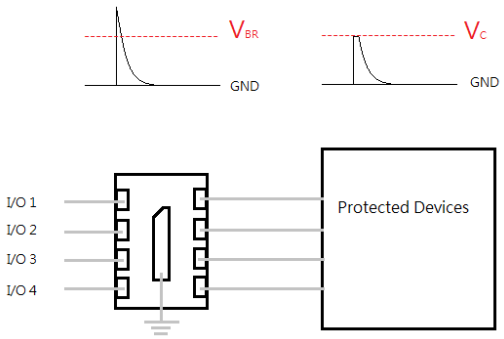


Figure 1

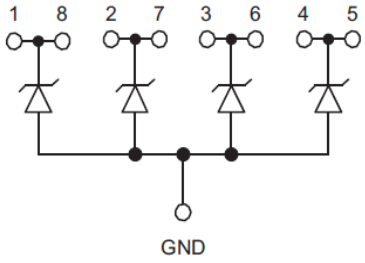


Figure 2

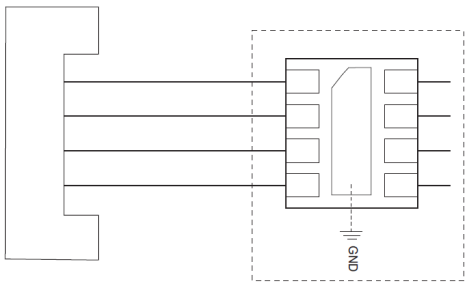


Figure 3

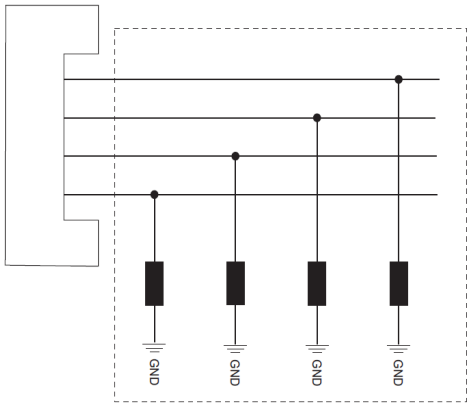


Figure 4