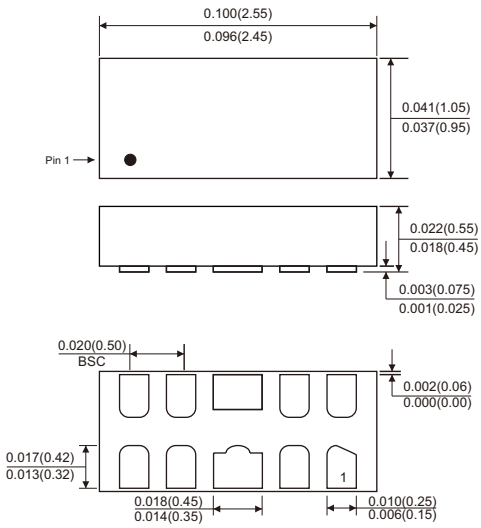
CPDWR101V5SBP-HF

RoHS Device
Halogen Free

Features

- Solid-state silicon-avalanche technology.
- Low clamping voltage.
- Low leakage current.
- IEC 61000-4-2 (ESD) ±15kV (air), ±12kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 4A (8/20μs)
- AEC-Q101 Qualified.

DFN2510-10L

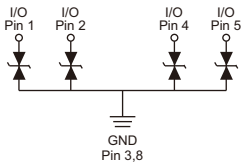


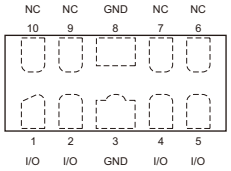
Dimensions in inches and (millimeter)

Mechanical data

- Case: DFN2510-10L, molded plastic.
- Mounting position: Any.

Circuit Diagram





Maximum Rating (at T_A=25°C unless otherwise noted)

Parameter	Conditions	Symbol	Value	Unit
Peak pulse power	T_P = 8/20μs	P_{PP}	16	W
Peak pulse current	T_P = 8/20μs	I_{PP}	4	A
ESD capability	IEC 61000-4-2(air) IEC 61000-4-2(contact)	ESD	±15 ±12	kV
Lead soldering temperature (10s)		T_L	260	°C
Operating junction temperature range		T_J	-55 to +125	°C
Storage temperature range		T_{STG}	-55 to +150	°C

Electrical Characteristics (at T_A=25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Working peak reverse voltage		V_{RWM}			1.5	V
Breakdown voltage	I_T = 0.1mA	V_{BR}	3			V
Reverse leakage current	V_{RWM} = 1.5V	I_R			0.1	μA
ESD Dynamic turn-on resistance	IEC 61000-4-2 0~+8kV, Contact mode, T=25°C	R_{DYN}		0.2		Ω
Clamping voltage	I_{PP} = 1A, T_P = 8/20μs	V_C		1.85	2.5	V
	I_{PP} = 4A, T_P = 8/20μs	V_C		3.2	4	
Junction capacitance	V_R = 0V, f = 1MHz, I/O to GND	C_J		0.3		pF
	V_R = 1V, f = 1MHz, I/O to GND	C_J		0.25	0.35	pF
	V_R = 0V, f = 1MHz, Between any I/O	C_J		0.13		pF

Notes: 1. The default test is I/O pin to ground.

2. The strong snap-back to a low holding voltage move into latch-up mode by an ESD event.
When designing the printed-circuit board (PCB), give careful consideration to impedance matching and signal coupling.
Do not connect the data lines to unlimited DC current sources like, for example, abattery, to avoid the device is “locked” in conducting mode.

Typical Rating and Characteristic Curves (CPDWR101V5SBP-HF)

Fig.1 - TLP

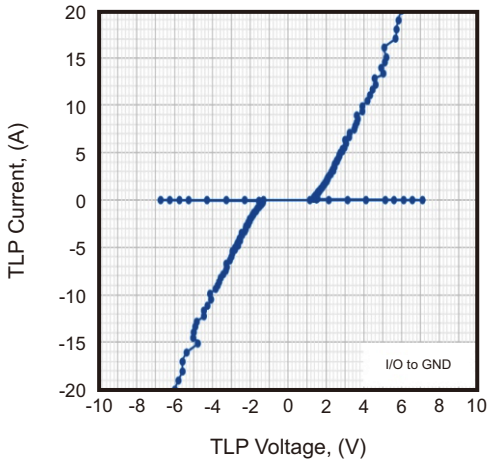


Fig.2 - Typical Variation of C_{IN} VS. V_{IN}

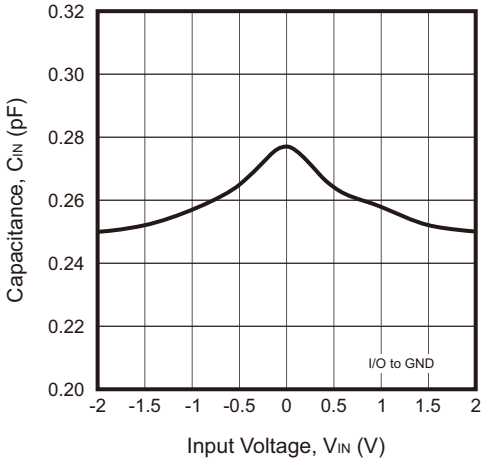


Fig.3 - Insertion loss S21

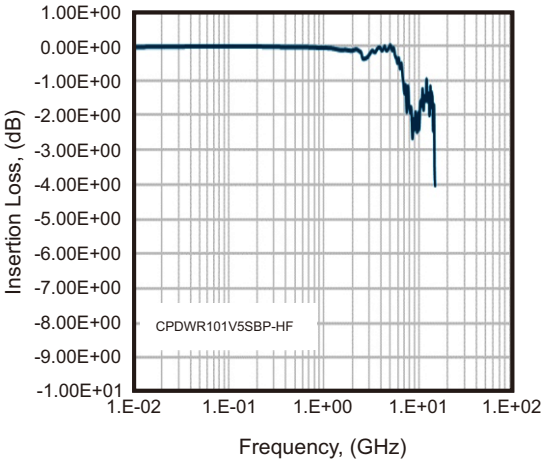


Fig.4 - IEC 61000-4-5 Surge 8/20μs

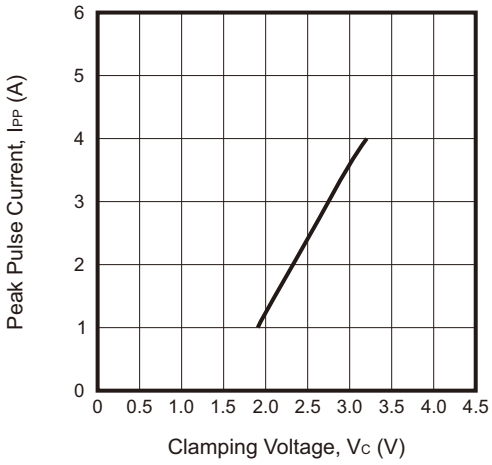
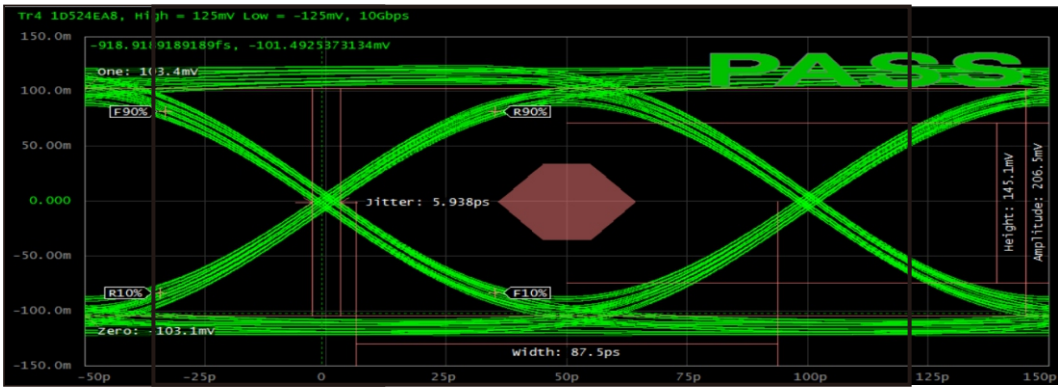
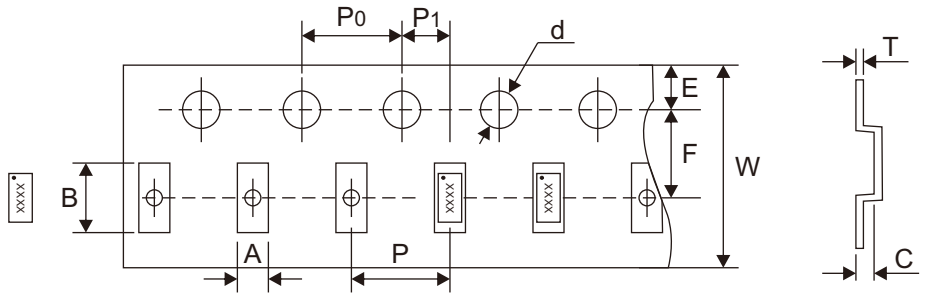
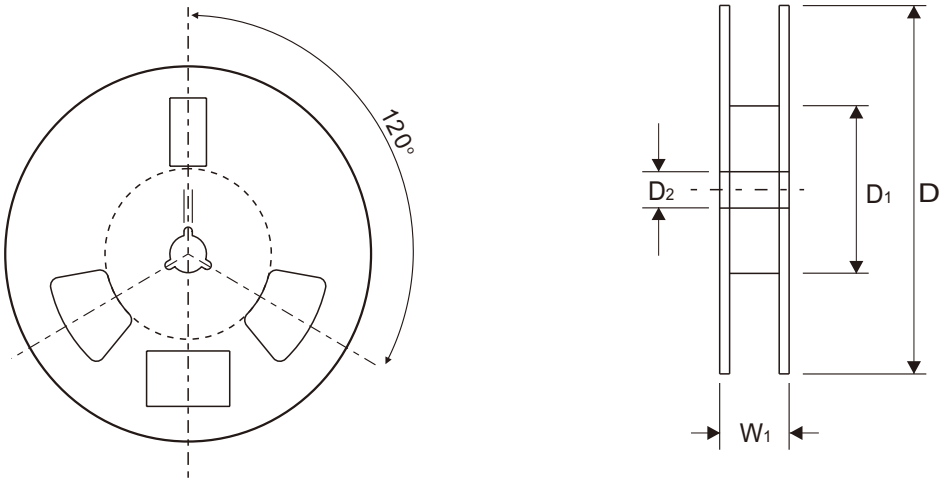


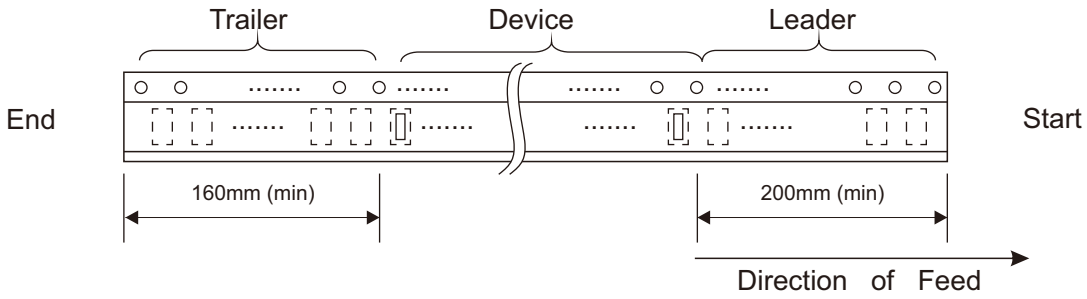
Fig.5 - USB 3.1 Gen 2 Eye Diagram with Device
(Data rate: 10Gbps)



Reel Taping Specification







	SYMBOL	A	B	C	d	D	D1	D2
DFN2510-10L	(mm)	1.20 ± 0.05	2.70 ± 0.05	0.70 ± 0.05	1.50 + 0.10 − 0.00	178.00 ± 1.00	54.50 ± 0.50	14.30 ± 0.20
	(inch)	0.047 ± 0.002	0.106 ± 0.002	0.028 ± 0.002	0.059 + 0.004 − 0.000	7.008 ± 0.039	2.146 ± 0.020	0.563 ± 0.008

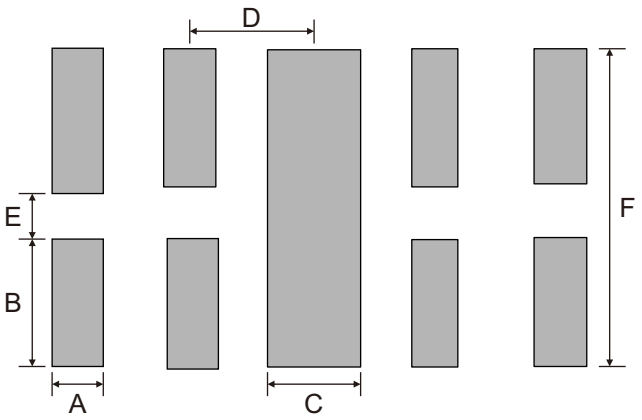
	SYMBOL	E	F	P	P0	P1	T	W	W1
DFN2510-10L	(mm)	1.75 ± 0.10	3.50 ± 0.05	4.00 ± 0.05	4.00 ± 0.05	2.00 ± 0.05	0.22 ± 0.03	8.00 + 0.30 − 0.10	12.40 ± 0.50
	(inch)	0.069 ± 0.004	0.138 ± 0.002	0.157 ± 0.002	0.157 ± 0.002	0.079 ± 0.002	0.009 ± 0.001	0.315 + 0.012 − 0.004	0.488 ± 0.020

Marking Code

Part Number	Marking Code
CPDWR101V5SBP-HF	1SN4

Suggested P.C.B. PAD Layout

SIZE	DFN2510-10L	
	(mm)	(inch)
A	0.20	0.008
B	0.60	0.024
C	0.40	0.016
D	0.50	0.020
E	0.20	0.008
F	1.40	0.055



Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
DFN2510-10L	3,000	7