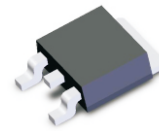


CMS35P03D-HF

P-Channel

RoHS Device

Halogen Free



Features

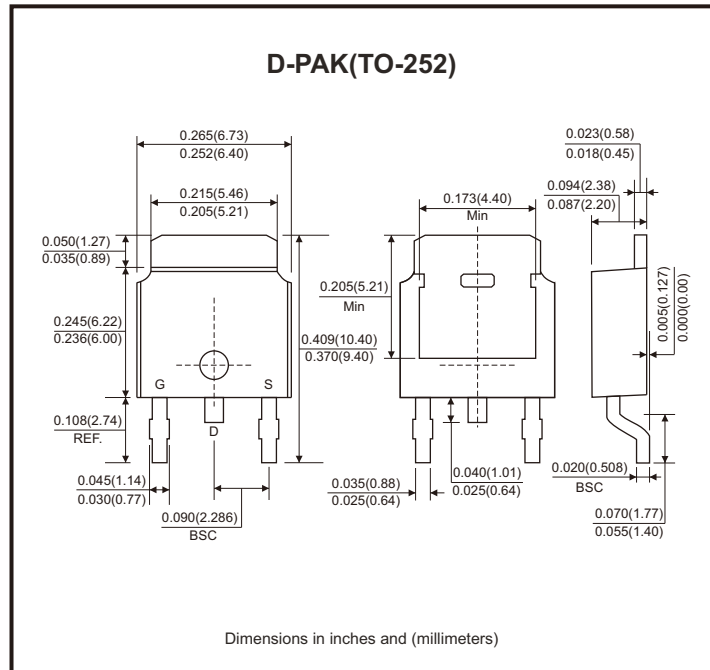
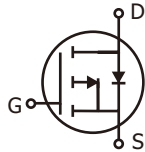
- Advanced high cell density trench technology.
- Super low gate charge.
- Excellent cdv/dt effect decline.
- Green device available.
- 100% EAS guaranteed.

Mechanical data

- Case: D-PAK/TO-252 standard package, molded plastic.

Circuit Diagram

- G : Gate
- S : Source
- D : Drain



Maximum Ratings

Parameter	Conditions	Symbol	Value	Unit
Drain-source voltage		V_{DS}	-30	V
Gate-source voltage		V_{GS}	± 20	V
Continuous drain current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	-35	A
	$T_C = 100^\circ\text{C}$	I_D	-22	
Pulsed drain current (Note 1, 2)		I_{DM}	-70	A
Continuous drain current (Note 1)	$T_A = 25^\circ\text{C}$	I_D	-8.5	A
	$T_A = 70^\circ\text{C}$	I_D	-6.8	
Total power dissipation (Note 4)	$T_C = 25^\circ\text{C}$	P_D	34	W
	$T_A = 25^\circ\text{C}$	P_D	2	
Single pulse avalanche energy, $L=0.1\text{mH}$ (Note 3)		E_{AS}	72	mJ
Single pulse avalanche current, $L=0.1\text{mH}$ (Note 3)		I_{AS}	38	A
Operating junction temperature range		T_J	-55 to +150	$^\circ\text{C}$
Storage temperature range		T_{STG}	-55 to +150	$^\circ\text{C}$
Thermal resistance junction-ambient (Note 1)	Steady state	$R_{\theta JA}$	62	$^\circ\text{C/W}$
Thermal resistance junction-case (Note 1)	Steady state	$R_{\theta JC}$	3.2	$^\circ\text{C/W}$

Electrical Characteristics (at $T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	BV _{DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.0		-2.5	
Forward transconductance	g _{fs}	V _{DS} = -5V, I _D = -10A		5		S
Gate-source leakage current	I _{GSS}	V _{GS} = ±20V			±100	nA
Drain-source leakage current (T _J =25°C)	I _{DSS}	V _{DS} = -30V, V _{GS} = 0V			-1	μA
Drain-source leakage current (T _J =55°C)		V _{DS} = -24V, V _{GS} = 0V			-5	
Static drain-source on-resistance (Note 2)	R _{DS(on)}	V _{GS} = -10V, I _D = -15A			25	mΩ
		V _{GS} = -4.5V, I _D = -10A			35	
Total gate charge (Note 2)	Q _g	I _D = -15A, V _{DS} = -15V, V _{GS} = -4.5V		12.5		nC
Gate-source charge	Q _{gs}			5.4		
Gate-drain ("miller") charge	Q _{gd}			5		
Turn-on delay time (Note 2)	t _{d(on)}	V _{DS} = -15V, V _{GS} = -10V I _D = -15A, R _G = 3.3Ω		4.4		nS
Rise time	t _r			11.2		
Turn-off delay time	t _{d(off)}			34		
Fall time	t _f			18		
Input capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		1345		pF
Output capacitance	C _{oss}			194		
Reverse transfer capacitance	C _{rss}			158		
Gate resistance	R _g	f = 1MHz		13		Ω
Source-drain diode						
Diode forward voltage (Note 2)	V _{SD}	I _S = -15A, V _{GS} = 0V, T _J =25°C			-1.2	V
Continuous source current (Note 1, 6)	I _S	V _G = V _D = 0V, Force current			-35	A
Pulsed source current (Note 2, 6)	I _{SM}				-70	A
Reverse recovery time	t _{rr}	I _F = -15A , T _J =25°C		12.4		nS
Reverse recovery charge	Q _{rr}	dI/dt = 100A/μs		5		nC
Guaranteed avalanche characteristics						
Single pulse avalanche energy (Note 5)	EAS	V _{DD} = -25V, L=0.1mH, I _{AS} = -17A	14.4			mJ

Notes: 1. The data tested by surface mounted on a 1 inch² FR-4 board with 2 oz copper.

2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

3. The EAS data shows max. rating. The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.1\text{mH}, I_{AS}=-38A$.

4. The power dissipation is limited by 150°C junction temperature.

5. The min. value is 100% EAS tested guarantee.

6. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Rating and Characteristic Curves (CMS35P03D-HF)

Fig.1 - Typical Output Characteristics

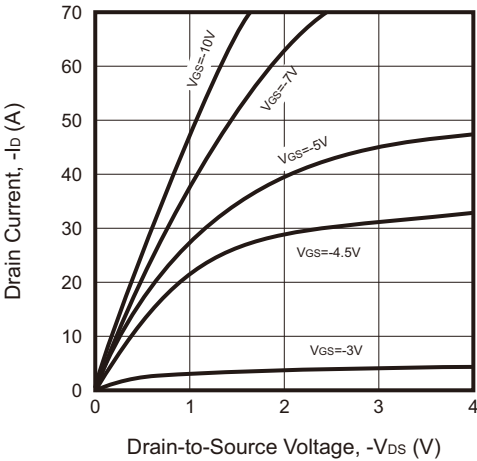


Fig.2 - On-Resistance vs. G-S Voltage

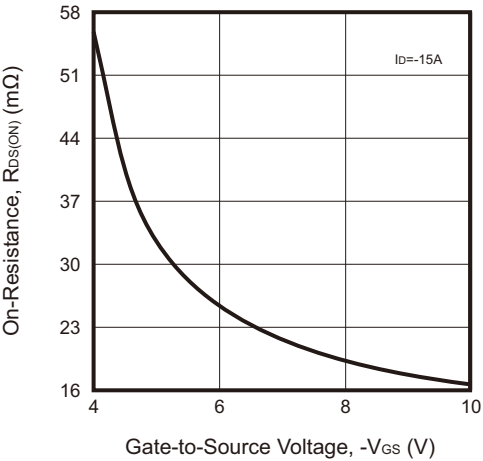


Fig.3 - Normalized $V_{GS(th)}$ vs. T_J

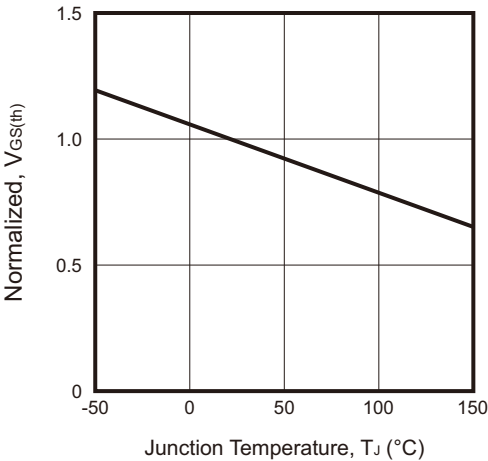


Fig.4 - Normalized $R_{DS(ON)}$ vs. T_J

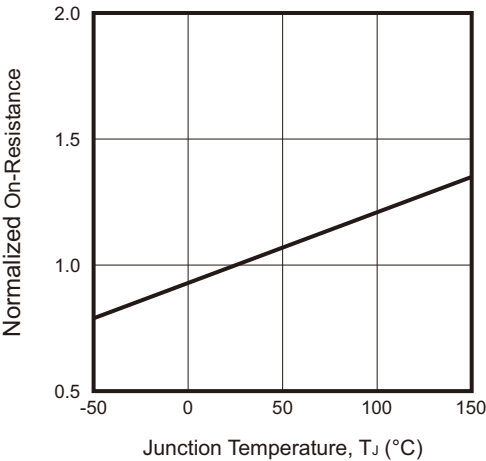


Fig.5 - Safe Operating Area

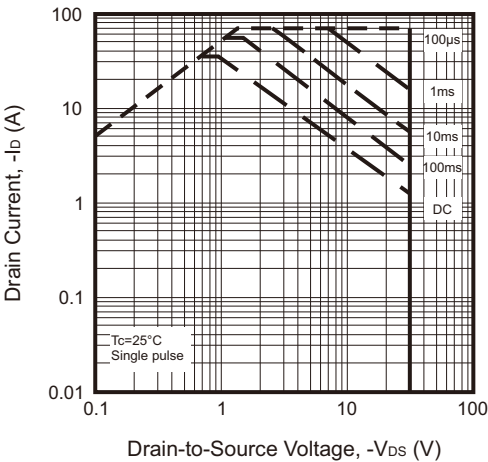
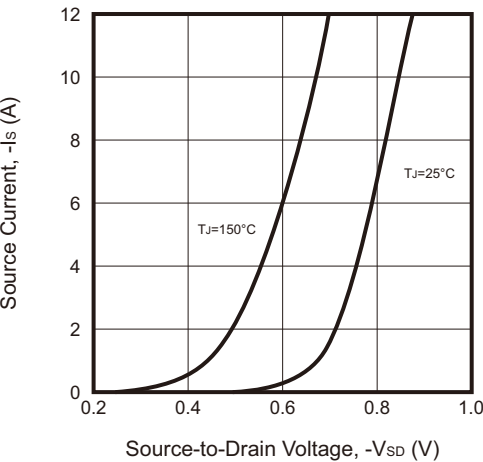


Fig.6 - Forward Characteristics of Reverse



Rating and Characteristic Curves (CMS35P03D-HF)

Fig.7 - Gate Charge Characteristics

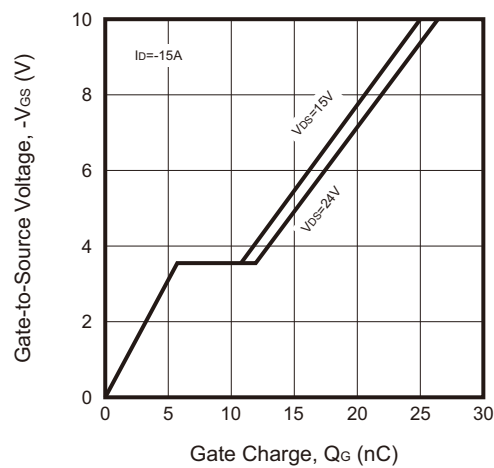
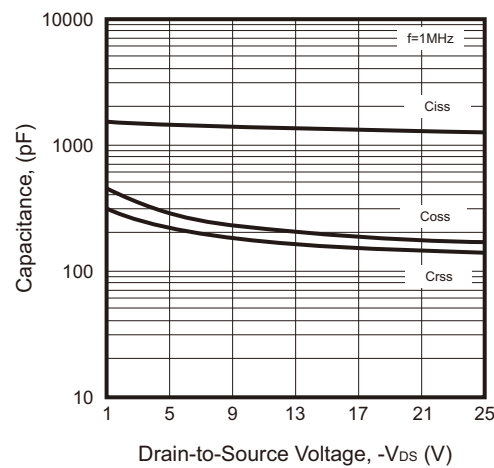
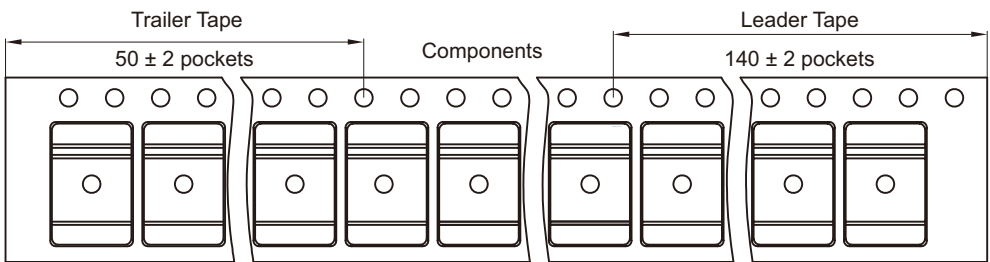
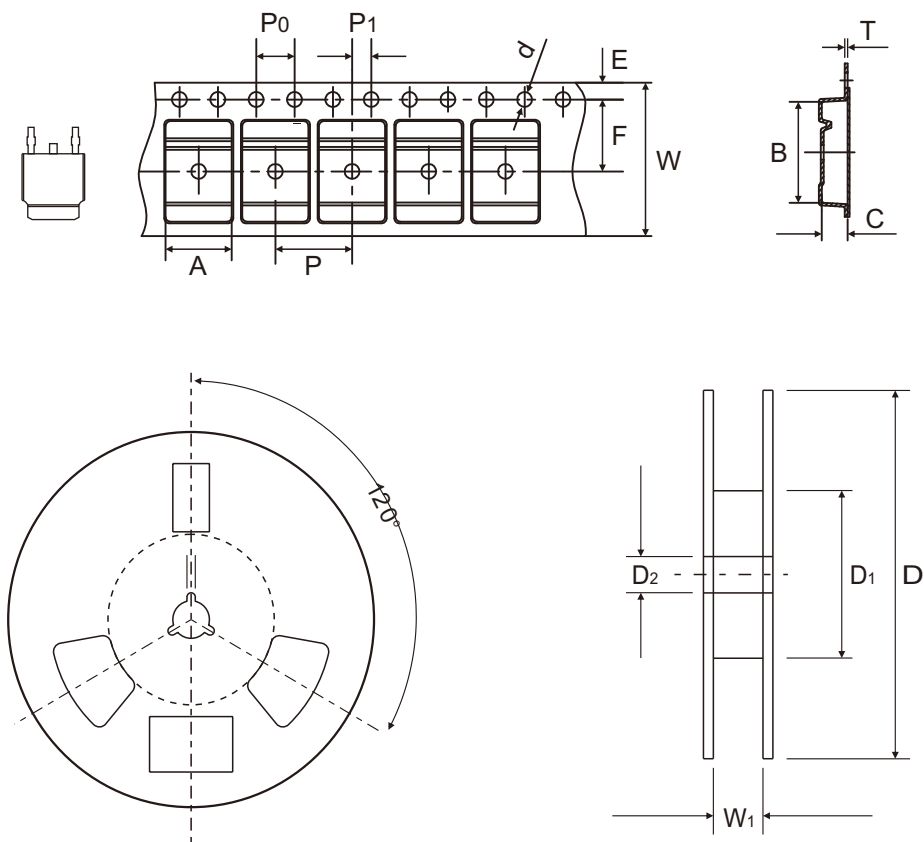


Fig.8 - Capacitance Characteristics



Reel Taping Specification

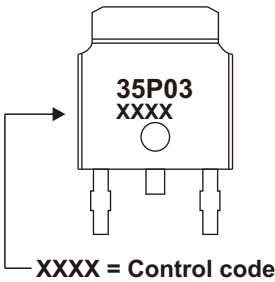


TO-252 (D-PAK)	SYMBOL	A	B	C	d	D	D1	D2
	(mm)	6.90 ± 0.10	10.50 ± 0.10	2.78 ± 0.10	1.50 ± 0.10	330 ± 1.00	100.00 ± 0.50	13.20 ± 0.20
	(inch)	0.272 ± 0.004	0.413 ± 0.004	0.109 ± 0.004	0.059 ± 0.004	12.992 ± 0.039	3.937 ± 0.020	0.520 ± 0.008

TO-252 (D-PAK)	SYMBOL	E	F	P	P0	P1	T	W	W1
	(mm)	1.75 ± 0.10	7.50 ± 0.10	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.10	0.25 ± 0.02	16.00 ± 0.10	16.40 ± 0.02
	(inch)	0.069 ± 0.004	0.295 ± 0.004	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.004	0.010 ± 0.001	0.630 ± 0.004	0.646 ± 0.01

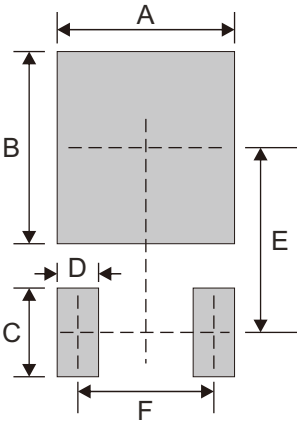
Marking Code

Part Number	Marking Code
CMS35P03D-HF	35P03



Suggested P.C.B. PAD Layout

SIZE	TO-252/D-PAK	
	(mm)	(inch)
A	6.00	0.236
B	6.50	0.256
C	3.00	0.118
D	1.40	0.055
E	6.25	0.246
F	4.60	0.181



Note: 1. The pad layout is for reference purposes only.

Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
TO-252/D-PAK	2,500	13