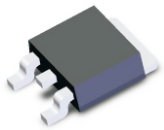
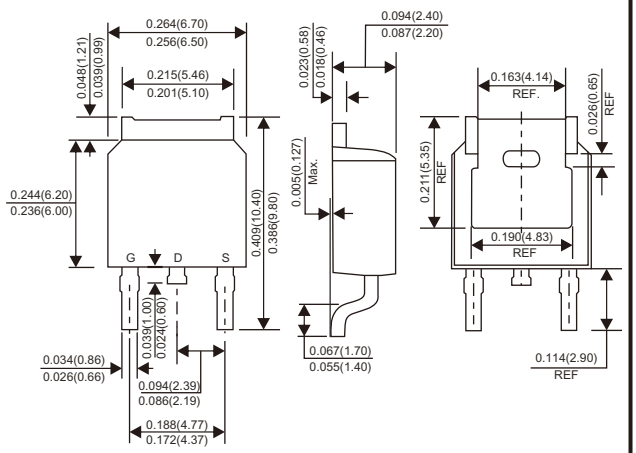
CMS23P04D-HF

P-Channel
RoHS Device
Halogen Free



D-PAK(TO-252)



Dimensions in inches and (millimeters)

Features

- Advanced high cell density trench technology.
- Excellent CdV/dt effect decline.
- Green device available.
- Super Low gate charge.
- 100% EAS Guaranteed.

Mechanical data

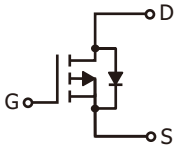
- Case: D-PAK/TO-252 standard package, molded plastic.

Description

The CMS23P04D is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications. The CMS23P04D meet the ROHS and Green Product require ment, 100% EAS guaranteed with full function reliability approved.

Circuit Diagram

- G : Gate
- D : Drain
- S : Source



Maximum Ratings (at T_A=25°C unless otherwise noted)

Parameter	Conditions	Symbol	Value	Unit
Drain-source voltage		V_{DS}	-40	V
Gate-source voltage		V_{GS}	±20	V
Continuous drain current (Note 1)	T_C = 25°C	I_D	-23	A
	T_C = 100°C	I_D	-18	
Pulsed drain current (Note 2)		I_{DM}	-46	A
Total power dissipation (Note 4)	T_C = 25°C	P_D	31.3	W
	T_A = 25°C	P_D	2	
Single pulse avalanche energy, L=0.1mH (Note 3)		E_{AS}	37	mJ
Single pulse avalanche current, L=0.1mH (Note 3)		I_{AS}	-27.2	A
Operating junction and storage temperature range		T_J, T_{STG}	-55 to +150	°C

Thermal Data

Parameter	Conditions	Symbol	Max. Value	Unit
Thermal resistance junction-ambient (Note 1)	Steady state	$R_{\theta JA}$	62	°C/W
Thermal resistance junction-case (Note 1)	Steady state	$R_{\theta JC}$	4	°C/W

Electrical Characteristics (at T_J=25°C unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain-source breakdown voltage	BV_{DSS}	-40			V	V_{GS} = 0, I_D = -250μA
Breakdown voltage temperature coefficient	$\triangle BV_{DSS}/\triangle T_J$		-0.012		V/°C	Reference to 25°C, I_D = -1mA
Gate threshold voltage	$V_{GS(th)}$	-1.0		-2.5	V	V_{DS} = V_{GS}, I_D = -250μA
Forward transconductance	g_{fs}		12.6		S	V_{DS} = -5V, I_D = -18A
Gate-source leakage current	I_{GSS}			±100	nA	V_{GS} = ±20V
Drain-source leakage current (T_J=25°C)	I_{DSS}			-1	μA	V_{DS} = -32V, V_{GS} = 0
Drain-source leakage current (T_J=55°C)				-5		V_{DS} = -32V, V_{GS} = 0
Static drain-source on-resistance (Note 2)	$R_{DS(on)}$		32	40	mΩ	V_{GS} = -10V, I_D = -18A
			52	65		V_{GS} = -4.5V, I_D = -12A
Total gate charge (Note 2)	Q_g		9		nC	I_D = -12A, V_{DS} = -20V, V_{GS} = -4.5V
Gate-source charge	Q_{gs}		2.54			
Gate-drain (“Miller”) change	Q_{gd}		3.1			
Turn-on delay time (Note 2)	$t_{d(on)}$		19.2		ns	V_{DD} = -15V, I_D = -1A, V_{GS} = -10V, R_G = 3.3Ω
Rise time	t_r		12.8			
Turn-off delay time	$t_{d(off)}$		48.6			
Fall time	t_f		4.6			
Input capacitance	C_{iss}		1004		pF	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz
Output capacitance	C_{oss}		108			
Reverse transfer capacitance	C_{rss}		80			
Guaranteed avalanche characteristics						
Single pulse avalanche energy (Note 5)	EAS	11.25			mJ	V_{DD} = -25V, L = 0.1mH, I_{AS} = -15A
Source-drain diode						
Diode forward voltage (Note 2)	V_{SD}			-1.2	V	I_S = -23A, V_{GS} = 0V, T_J = 25°C
Continuous source current (Note 1, 6)	I_S			-23	A	V_G = V_D = 0V , Force current
Pulsed source current (Note 2, 6)	I_{SM}			-46	A	

Notes: 1. Surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%.
3. The EAS data shows Max. rating. The test condition is VDD=-25V, VGS=-10V, L=0.1mH, IAS=-27.2A.
4. The power dissipation is limited by 150°C junction temperature.
5. The min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

Rating and Characteristic Curves (CMS23P04D-HF)

Typical Characteristics

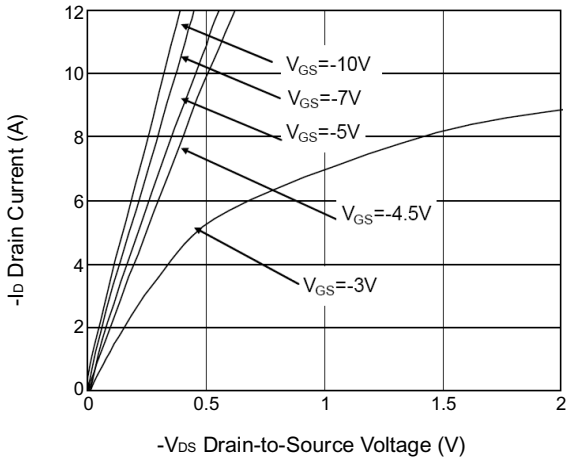


Fig.1 Typical Output Characteristics

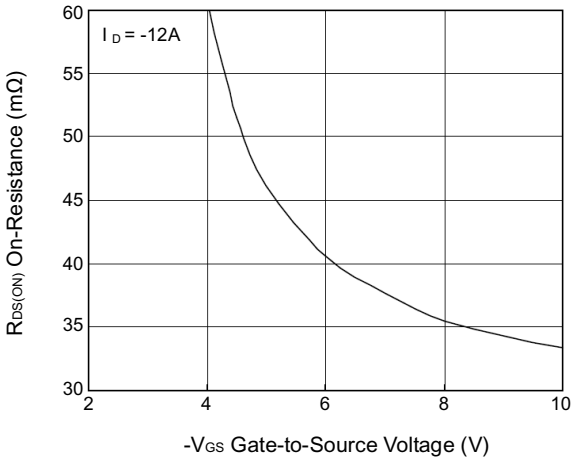


Fig.2 On-Resistance vs. G-S Voltage

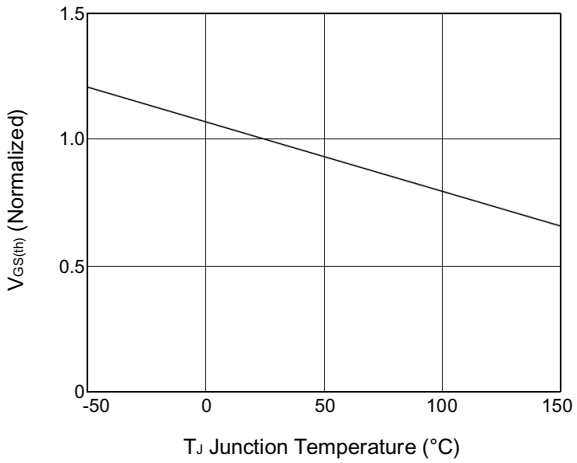


Fig.3 Normalized $V_{GS(th)}$ vs. T_J

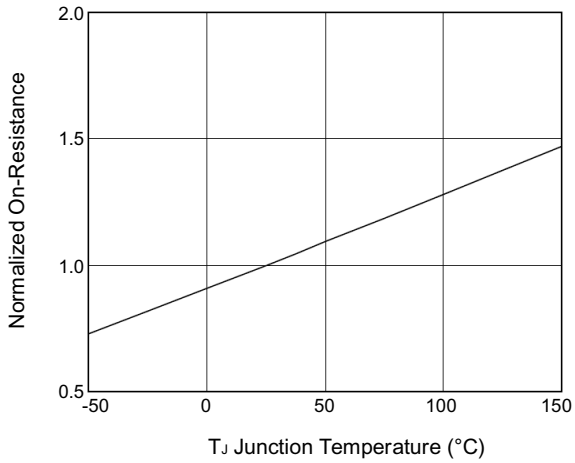


Fig.4 Normalized $R_{DS(ON)}$ vs. T_J

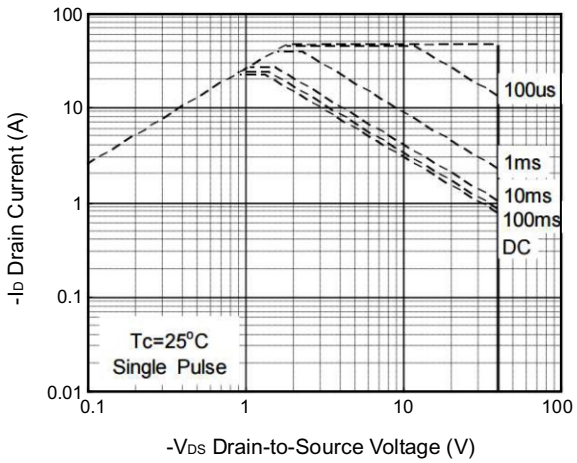


Fig.5 Safe Operating Area

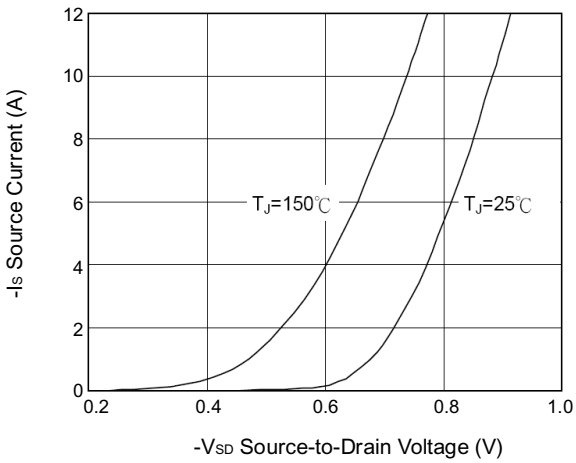


Fig.6 Forward Characteristics of Reverse

Rating and Characteristic Curves (CMS23P04D-HF)

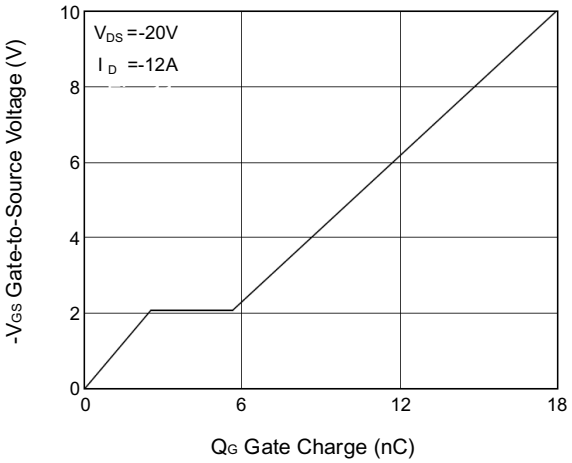


Fig.7 Gate Charge Characteristics

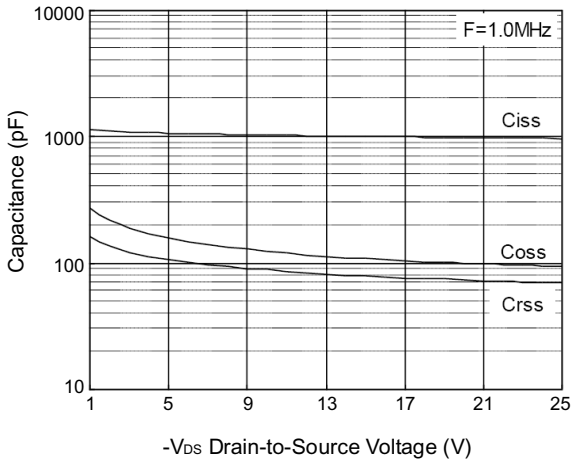


Fig.8 Capacitance Characteristics

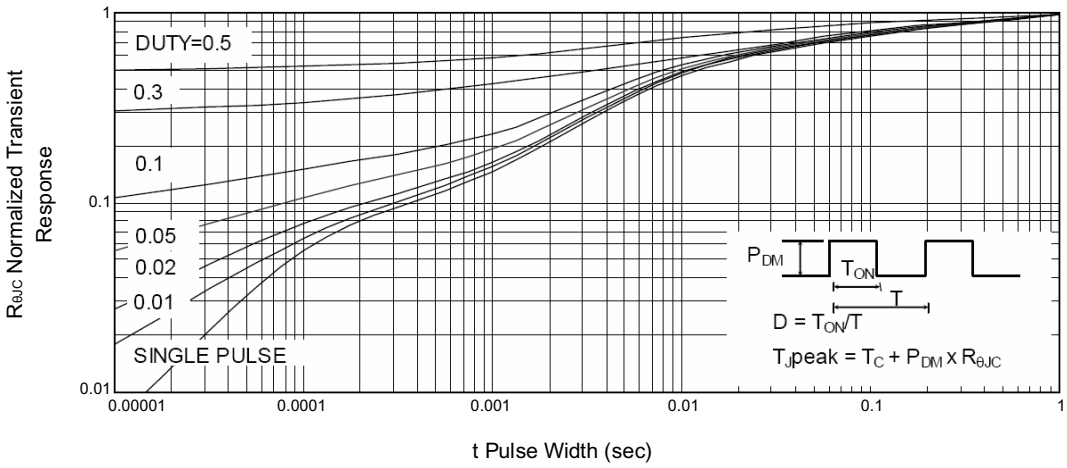


Fig.9 Normalized Maximum Transient Thermal Impedance

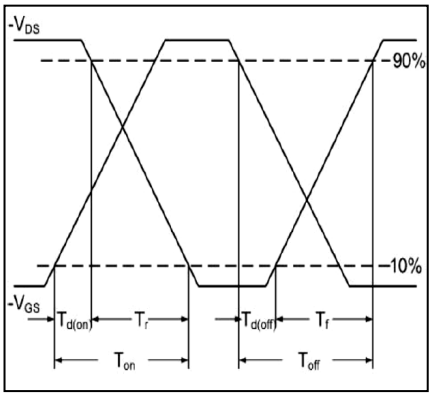


Fig.10 Switching Time Waveform

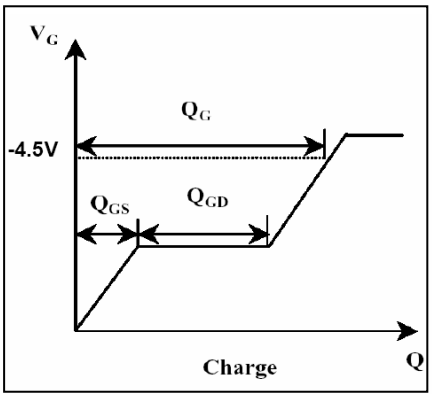
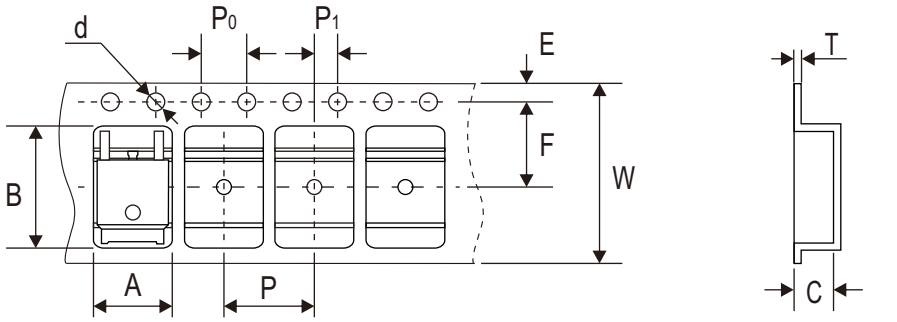
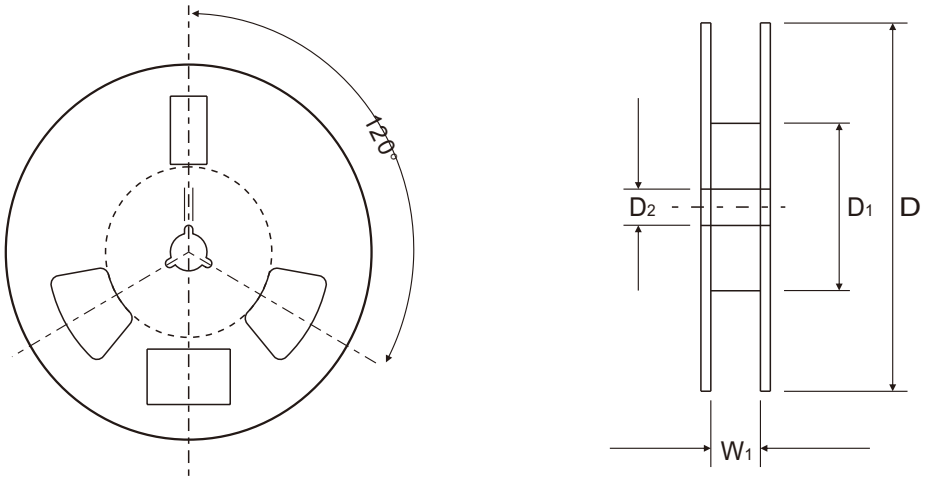
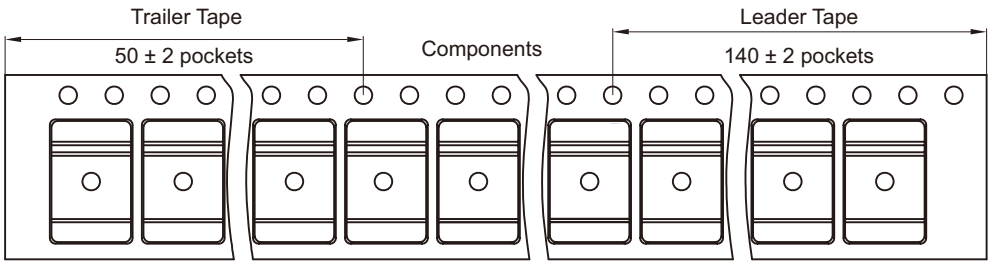


Fig.11 Gate Charge Waveform

Reel Taping Specification





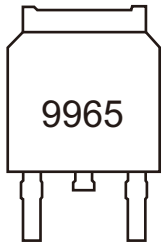


	SYMBOL	A	B	C	d	D	D1	D2
TO-252 (D-PAK)	(mm)	6.90 ± 0.10	10.50 ± 0.10	2.78 ± 0.10	1.50 ± 0.10	330 ± 1.00	100.00 ± 0.50	13.20 ± 0.20
	(inch)	0.272 ± 0.004	0.413 ± 0.004	0.109 ± 0.004	0.059 ± 0.004	12.992 ± 0.039	3.937 ± 0.020	0.520 ± 0.008

	SYMBOL	E	F	P	P0	P1	T	W	W1
TO-252 (D-PAK)	(mm)	1.75 ± 0.10	7.50 ± 0.10	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.10	0.25 ± 0.02	16.00 ± 0.10	16.40 ± 0.02
	(inch)	0.069 ± 0.004	0.295 ± 0.004	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.004	0.010 ± 0.001	0.630 ± 0.004	0.646 ± 0.01

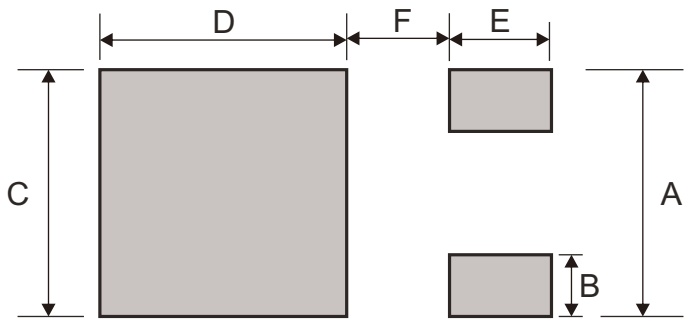
Marking Code

Part Number	Marking Code
CMS23P04D-HF	9965



Suggested P.C.B. PAD Layout

SIZE	TO-252 / DPAK	
	(mm)	(inch)
A	6.17	0.243
B	1.60	0.063
C	5.80	0.228
D	6.20	0.244
E	3.00	0.118
F	2.58	0.101



Note: 1. The pad layout is for reference purposes only.

Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	REEL SIZE (inch)
TO-252/D-PAK	2,500	13